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"Gallium-based Solid Liquid Interdiffusion Bonding of Semiconductor Substrates near room temperature “

Joerg Froemel

The dissertation compromises 120 pages and contains 80 figures, 19 tables, and 92 references.

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Abstract:

Within this work, bonding technologies based upon the alloying of gallium with other metals to assemble semiconductor substrates for the possible application of encapsulation and 3D-integration of micro systems and devices have been researched. Motivated by the important demand to achieve low temperature processes, methods with bonding temperatures below 200°C were investigated. Necessary technologies like the deposition of gallium as thin film and subsequent micro structuring have been developed. The alloying between gallium and gold as well as gallium and copper was analysed in detail. A good correlation between the elemental composition of the interface and its mechanical and electrical parameters was established, particularly regarding its thermal dependence. It emerged that in case of combination Au/Ga Kirkendall void are extensively formed whereby serious problems with mechanical strength as well as hermeticity emerged. In case of Cu/Ga, this problem is existent to a much lesser degree; it was possible to create hermetic tight bonds. For the necessary pre-treatment of copper, several methods could be successfully demonstrated. In summary, the development of bonding technologies based upon metallic interfaces that exhibit electric conductance, high strength and hermetic seal could be demonstrated.

Keywords:

Waferbonding
Alloying
SLID (Solid Liquid Interdiffusion)
Gallium
Bond interfaces
Intermetallic phases

Bibliographische Beschreibung:

"Gallium basiertes Solid Liquid Inter-Diffusion Fügen von Halbleitersubstraten nahe Raumtemperatur“

Jörg Frömel

Die Dissertation umfasst 120 Seiten, es sind 80 Abbildungen, 19 Tabellen und 92 Literaturstellen enthalten.

Technische Universität Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Dissertation 2015

Referat:

In dieser Arbeit werden Bondverfahren zum Fügen von Halbleitersubstraten für mögliche Anwendungen für die Verkapselung und 3D-Integration von Bauelementen der Mikrosystemtechnik erforscht, die auf der Legierungsbildung von Gallium mit anderen Metallen beruhen. Motiviert von der zentralen Anforderung an niedrige Prozesstemperaturen wurden Methoden mit Fügetemperaturen deutlich unter 200°C untersucht. Dafür nötige Technologien zum Abscheiden von Gallium als Dünnschicht und das anschließende Mikrostrukturieren wurden entwickelt. Die Legierungsbildung zwischen Gallium und Gold sowie zwischen Gallium und Kupfer wurde im experimentell im Detail analysiert. Dabei konnte eine gute Korrelation zwischen der stofflichen Zusammensetzung und den mechanischen bzw. elektrischen Parametern der Zwischenschicht, auch und insbesondere hinsichtlich ihrer Temperaturabhängigkeit gefunden werden. Es stellte sich heraus, dass im Falle der Kombination Au/Ga Kirkendall Hohlräume in einer Menge entstehen, die zu erheblichen Problemen bezüglich mechanischer Festigkeit und Dichtheit der Fügeverbindung führen. Bei der Materialkombination Cu/Ga hingegen trat dieses Problem nur begrenzt auf; es war möglich hermetisch dichte Verbindungen herzustellen. Für die bei Kupfer nötige Vorbehandlung wurden mehrere Methoden erfolgreich getestet. Insgesamt konnte die Entwicklung von Fügetechnologien gezeigt werden, die metallische Zwischenschichten verwenden, elektrisch leitfähig sind, sehr gute Festigkeiten aufweisen und hermetisch dicht sind.

Stichwörter:

Waferbonden
Legierungsbildung
SLID (Solid Liquid Inter-Diffusion)
Gallium
Fügeverbindung
Intermetallische Phasen

Content

Inhaltsverzeichnis

List of abbreviations

AIMR	Advanced Institute for Materials Research
BDRIE	Bonding and Deep Reactive Ion Etching
EDX	Electron Dispersive X-ray
EDXA	Electron Dispersive X-ray Analysis
EVG	EV Group
FET	Field Effect Transistor
FIB	Focused Ion Beam
FT-IR	Fourier-Transform Infrared
ICP	Inductively Coupled Plasma
MEMS	Micro Electro Mechanical Systems
PVD	Physical Vapour Deposition
RADAR	Radio Detection and Ranging
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
SLID	Solid Liquid Interdiffusion
SOI	Silicon on Insulator
TLP	Transient Liquid Phase
UV	Ultra-Violet
WPI	World Premier International Research Centres Initiative

Preface and Acknowledgements

During recent decades, waferbonding for semiconductor devices has entered micro devices production as a standard process. While a very small portfolio of available bonding technologies initially existed, now a multitude of different methods is available. This development has been driven by the ever-increasing number of different substrate materials and functional materials that become available for fabrication. On the other hand, this material variety in itself enables the development of new methods and technologies. During my work at the Fraunhofer Institute for Electronic Nano Systems in Chemnitz, Germany, the need for low temperature bonding processes was apparent, as input by numerous industrial partners as well as from the scientific community. At the same time, I was lucky to cooperate with the renowned Advanced Institute for Materials Research (AIMR) of the World Premier International Research Centres Initiative (WPI) at Tohoku University Sendai, Japan, including several long stays as a visiting scientist. The AIMR is specialised in material development and characterisation. This unique combination of application-oriented research at Fraunhofer and high-level basic material knowledge at AIMR provided me with the opportunity and inspiration to pursue the goal of developing a very low temperature wafer bonding technology based upon a material (gallium) that has not been used to date in the field of micro devices fabrication.
I would like to thank all persons who have helped me during the time of my dissertation with words and deeds and thus contributed to the success of this work.

I would particularly like to thank:

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1. Introduction

Micro systems technology is a direct evolution from semiconductor microelectronics. Microelectronics originally started by realisation of the field effect transistor. After a patent applied in 1925 (Lilienfeld, 1925) describing the principle of a semiconductor amplifier, the first field effect transistor (FET) with insulated gate was demonstrated and patented (Heil, 1934) about 10 years later, in 1934. In the 1940s, many activities took place to demonstrate a working semiconductor amplification device with better performance than cathode ray tubes, as well as for replacing relays. This was driven by the need to improve Radio Detection and Ranging (RADAR) devices and electronic calculators used in the ongoing war. Therefore, it is unsurprising that the main actors in this research have been Telefunken in Germany and Bell Labs in the USA. In 1945, Mataré and Welker in Germany (working on a "Duodiode") as well as Shockley and Brattain in the USA demonstrated their working FET. The performance of this FET was much worse than expected (Shockley, 1976). Based upon remaining documents from the supervisor of Shockley of Bell Labs made at the time of their research, it is known that the results were most likely based upon repetition of the work of Lilienfeld (Arns, 1998).
In December 1947, Shockley, Bardeen and Brattain claimed the invention of another type of transistor, namely the bipolar transistor. In August 1948, Mataré and Welker, who moved to the French company Freins & Signaux Westinghouse after the war, patented their bipolar transistor, at that time called "Transistron". Later, Shockley and his co-workers were awarded the Nobel Prize of Physics for inventing the diffusion transistor. The previously mentioned investigators tried to use silicon as the semiconductor material for the devices, although they failed at that time. Instead they succeeded by using germanium. Later from 1954 (Texas Instruments and Bell Labs), silicon started to replace germanium due to the possibility to use the good isolation properties of the very stable silicon dioxide. Nowadays, beside power and high frequency applications, silicon is the major material for microelectronic devices.

Following soon after the discovery of the piezoresistive effect in 1954 in silicon and germanium, the first mechanical devices using semiconductor inherent properties, namely pressure sensors, were made (Tufte, et al., 1963). With the resonant gate, transistor devices using parts vibrating at a high frequency made their debut (Nathanson, et al., 1967). Another class of micro devices, chemical sensors, started to surface about 10 years later (Esashi, et al., 1978). Since that time, micro systems have evolved, developed and spread in many ways. In the decades that followed the practical invention of semiconductor micro technology, many key technologies that enabled further possibilities have been developed, such as the Reactive Ion Etching (RIE) of silicon. Another such key technology is the semiconductor wafer bonding.

1.1 Semiconductor wafer bonding in micro technology

Semiconductor wafer bonding soon emerged after the processing of microelectronic products on wafer scale started. Nevertheless, before that time, high precision bonding processes had already been developed. In 1734, it was noticed and used that well-polished surfaces stick together. (Desaguliers, 1734). Much later, this effect was used to fabricate optical devices. (Lord Rayleigh, 1934) This could be seen as the starting point of direct bonding. The 60ths of the last century were characterised by many discoveries in the field of semiconductor bonding. This was driven by the need to find a suitable packaging method for the recently developed microelectronic devices. In the previous decade, transistors were packaged in the same glass bulbs like cathode ray tubes, given that the lack of a suitable packaging that could take advantage of the smaller size of the transistors. From that time onwards, solid liquid interdiffusion (SLID) bonding from Fairchild Semiconductor (Bernstein, et al., 1966) and anodic bonding from P. R. Mallory &- Co. Inc. (Wallis, et al., 1969) are still used in industrial applications today. Much later the now also common silicon direct bonding has been discovered (Lasky, 1986), (Shimbo, et al., 1986), including the low temperature variants (Kissinger, et al., 1991), (Goesele, et al., 1995). In this century, most remarkable process in wafer bonding technologies has been made among others thus far in the field of glass frit bonding (Knechtel, et al., 2006), metal thermo-compression bonding (Froemel, et al., 2011) and reactive bonding (Braeuer, et al., 2012).

Semiconductor wafer bonding technologies play an important role mainly in three application fields: substrate fabrication (e.g. SOI), functional element fabrication (e.g. bulk micromechanics) and wafer level packaging (capping). Therefore, they are indispensable parts of today's technology portfolio.

There are different possible ways to classify semiconductor wafer bonding technologies. For this thesis, it was chosen to use the bonding mechanism as classification element. (Figure 1) On the one hand, the bonding technologies are based upon chemical bonds, namely anodic bonding and silicon direct bonding. Silicon direct bonding has two low temperature variants, Surface Activated Bonding and plasma activated bonding. In the field of diffusion-based methods, we can see liquid and solid state technologies. A typical example of solid state bonding is thermo-compression bonding, whereas for liquid state it is eutectic bonding. SLID bonding is partly liquid and partly solid state diffusion-based.

Interestingly the first developed methods (e.g. SLID and anodic bonding) are being done at relatively low temperatures (~200-400°C) and subsequently the era of high temperature bonding processes (silicon direct bonding) started. The low temperature processes became interesting again with the emergence of use of heterogeneous materials in MEMS, the thermal budget limitations of LSI in 3D-Integration and high precision sensors.

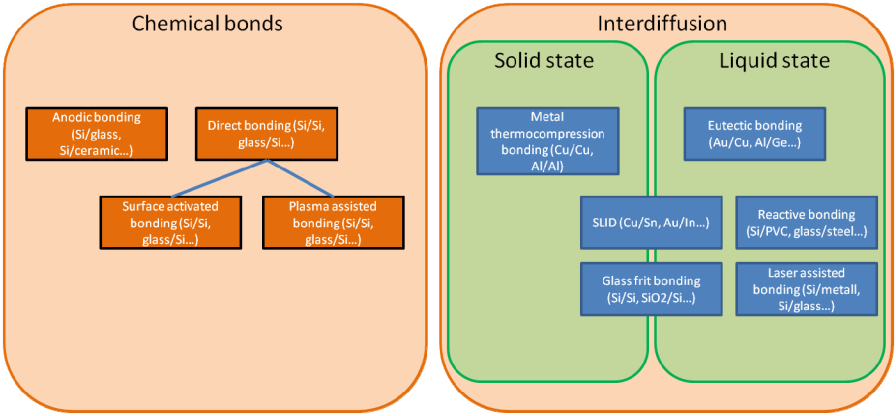


Figure 1. Selected bonding technologies overview, minor variants resulting from different surface pre-treatments is not included

1.2 Need for low temperature processes

When assembling heterogeneous materials, which is often the case in the field of packaging of micro devices on wafer level, thermo-mechanical stress is a serious problem. At the very beginning of MEMS technology, only one material as a substrate, mainly silicon, has been used. However, very soon with the appearance of borosilicate glass the first heterogeneous systems consisting of silicon and glass have been fabricated. With the desire to develop such systems the problem of using materials with different thermal mechanical behaviour that was already well known in mechanical engineering also entered the field of MEMS. The reason for this being problematic is the difference in thermal expansion coefficient. In the following special borosilicate glass was developed to match the thermal expansion coefficient of silicon as much as possible. Due to different thermal expansion coefficients of the used materials, the assembly process that is usually done at elevated temperatures (e.g. 400°C) generates a significant amount of thermo-mechanical stress. This stress not only negatively influences device characteristics, but also reduces reliability and lifetime due to the additional strain that it causes in the bond areas of the heterogeneous device (Royes, 1988). Especially in the field of micro system technology that uses many different materials, a need to develop ways to avoid this thermo-mechanical stress exists. One way to avoid is to use assembly processes that do not require elevated temperature and working near room temperature. Nonetheless, this bonding technology should enable high fracture toughness of the bond, hermetic sealing and should still be economic.

The linear thermal expansion coefficient α is determining the change in dimension Δl of a given part with change of temperature ΔT. It is specific for every material.

$$\Delta l = \alpha \Delta T \qquad 1$$

In the case of homogeneous material the change in one dimension, for example length or thickness can be calculated according to formula 1. When materials with different thermal expansions coefficients are used in one system, it will be different for the same change of temperature for each material. This difference in thermal expansion will cause thermo-mechanical stress. The higher the difference of the thermal expansion coefficient the higher is the thermo-mechanical stress. It is well known that thermo-mechanical stress is detrimental to the lifetime of a system. When considering bonding, ΔT is the difference between bonding temperature T_{bond} and application temperature T_{app}.

$$\Delta T = T_{app} - T_{bond} \qquad 2$$

In case of a bimorph (two different materials bonded together), the deformation caused by the thermo-mechanical stress can be calculated by equilibrium of forces and moments in the cross section (Mehner, 1994).

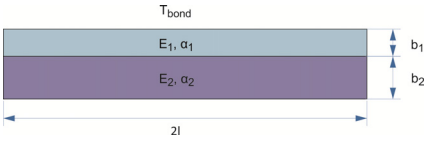


Figure 2. Bimorph system of two bonded materials, E = Young's Modulus, α = linear thermal expansion coefficient, 2l = lengths, b = thickness

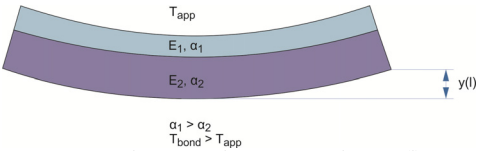


Figure 3. Bimorph system with temperature change, y(l) = deformation

$$y(l) \cong \frac{l^2}{2r} \qquad 3$$

In a situation depicted by Figure 2 and Figure 3 the radius of deformation is calculated by:

$$r = \frac{b_1 + b_2}{6} \frac{3\left(1 + \frac{b_1}{b_2}\right)^2 + \left(1 + \frac{b_1 E_1}{b_2 E_2}\right)\left[\left(\frac{b_1}{b_2}\right)^2 + \frac{b_2 E_2}{b_1 E_1}\right]}{\Delta\alpha \cdot \Delta T \left(1 + \frac{b_1}{b_2}\right)^2} \qquad 4$$

It can easily be recognised that to make *y(l)* small, $\Delta\alpha$ and ΔT should be as small as possible. The linear thermal expansion coefficient is given as a material characteristic. Whereas for some materials it is possible to adjust it (as has been done with borosilicate glass that has been matched to silicon), for most functional material, e.g. piezo-electric materials, it remains difficult. On the other hand, reducing the difference between bonding temperature and application temperature is mainly a matter of technology and can be applied for many different materials.
Several micro technologies materials suppliers have engaged significant effort to develop materials that match the thermal expansion coefficient of silicon, the most used material for micro systems today. For example, special glass substrates or glass pastes (Knechtel, et al., 2006). But material variety has increased so much in recent years. There are also now many materials in use that cannot withstand higher temperatures, including polymers, biologic active substances for lab-on-chip, and magnetic materials (Curie temperature). To allow this material variety to be used, bonding processes that keep substrate temperature near room temperature are strongly needed. There are many research activities around the world by different groups, with Table 1 showing a representative selection.

Table 1: Overview of currently applied wafer bond technologies that operate near room temperature (substrate temperature)

bonding technology	**limitations in application**
reactive bonding (Braeuer, et al., 2012)	problem of connecting different reaction areas not fully solved requires complex deposition process
nanoporous gold (Oppermann, et al., 2012)	difficult to achieve hermeticity
surface activated bonding (Higurashi, et al., 2009)	requires very flat surfaces needs to be done in ultra high vacuum
atomic diffusion bonding (Kon, et al., 2013)	requires very flat surfaces
laser assisted bonding (Tan, et al., 2005)	time consuming sequential process bond substrate must be transparent in laser wavelength

Although there has been remarkable progress in development of such near room temperature processes, still there are limitations in their applicability.

What is still needed is a wafer bonding technology combines all advantages:

- simple deposition process
- high bonding strength
- good hermeticity
- ability for electrical contact to allow application in 3D-Integration
- insensibility to surface roughness of substrates

One possible solution is the application of SLID bonding with new materials with extremely low melting point. Such a material is gallium, for example. In the further part of this work, gallium-based SLID bonding will be investigated. This entirely new technology has not yet been applied for semiconductor wafer bonding.

2. Sample preparation

For useful application, several key processes have to be checked, modified or developed. These processes include gallium deposition, micro structuring of the gallium thin film and the wafer bonding process itself. The key point is the very low melting point of the gallium of 30°C. Many available processes in MEMS and micro technology require temperatures higher than room temperature. As an example, sputtering shall be mentioned. During sputtering, the impact of the sputtered material ions on the substrate is partly transformed to heat, increasing the temperature of the substrate. To have an applicable technology process for gallium, it is required to keep the substrate temperature from deposition until final alloying below the melting of 30°C at all times. Otherwise the metal would simply become liquid on the substrate with uncontrollable behaviour that cannot be accepted in a productions scenario that require repeatability and a certain yield. To achieve the ability to keep the temperature below melting point the available technologies have to be modified accordingly.

2.1 Deposition of gallium thin films

Deposition of the gallium thin films is the first step in the series of processes required for the SLID bonding. In this work film with thicknesses ranging from several 100nm to several µm are regarded as thin film. As per the state of the art, essentially three different deposition methods are possible. This includes PVD (physical vapour deposition), thermal decomposition of GaN and electroplating.

2.1.1 Physical vapour deposition

The physical vapour deposition can approximately be separated into two fields, namely evaporating and sputtering. The main difference between these processes is that in case of evaporating the material is simply heated up until a significant part of it evaporates. This vapour is not especially directed onto a substrate and only condenses every surface that it reaches that is cold enough. The most common source for heating the material is a high-energy electron beam.

By contrast, sputtering ionizes the metal vapour and creates plasma by using an electromagnetic field. This field is directed from the target surface to the sample surface, therefore accelerating the metal ions until they hit the sample surface and recombine to form a film on the sample. The kinetic energy of the ions impact is creating a considerable heat depending on the electrical power.

For gallium, both sputtering and evaporation have already been successfully shown. (Jezequel, et al., 1977) Nevertheless, there are some difficulties connected to this. For

evaporating, it is natural that the target material becomes liquid during the process. The equipment is built in a way that the crucibles are in face up configuration so that the melt remains inside the crucible. In the case of sputtering, the target usually does not become liquid during the process. Most common sputter equipment has the targets horizontally face down or vertically build in. Due to the very low melting point of gallium, even in the case the target would be cooled, at least the surface becomes liquid. This is why only special equipment with face up target holder that can hold liquid targets can be used.
Another difficulty is that the PVD deposited gallium immediately forms droplet like structures on the surface of the substrate rather than a homogeneous thin film. The only known way to prevent this is the cooling of the substrate to temperatures as low as -160°C during deposition. (Berwian, 2005)
To conclude gallium can be successfully deposited by PVD processes, although the effort is relatively high due to specialised equipment that allows liquid targets and can cool the substrate to cryogenic temperatures is necessary.

2.1.2 Thermal decomposition GaN

Another possibility to create gallium thin films on semiconductor is the dissociative evaporation of GaN. If this technique would be applicable, deposition of a GaN film and subsequent annealing to dissolve and evaporate the nitrogen could be used to create gallium films. Since gallium nitride is a semiconductor material with a large direct band gap, it is interesting for application in the field of short wavelength photonic devices. Due to this interest, its properties, like thermal stability, have been investigated in detail. For this reason, the thermal decomposition effect is well known. The decomposition process heavily depends on the parameters. Especially the environmental gas is important.
In the case of temperature treatment under vacuum conditions, the reaction can be described as follows:

$$GaN\,(s) \rightarrow Ga\,(g) + 0.5N + 0.25\,N_2 \qquad 5$$

This decomposition requires high temperatures of at least 1100K and the gallium is produced in its vapour phase. Essentially the same behaviour can be found by annealing under argon, helium and nitrogen atmosphere.
The dissolution process is significantly different by using hydrogen gas. In this case, the reaction changes to:

$$GaN\,(s) + 1.5\,H_2 \rightarrow Ga\,(g) + NH_3 \qquad 6$$

The decomposition already starts at 873K. Nevertheless, gallium is also produced in its vapour phase. In both cases, the equilibrium partial pressure of gallium is higher than the saturated vapour pressure. Due to this, the gaseous gallium is immediately condensing on the GaN surface and forming a liquid layer there. (L'vov, 2000)

For this result, it is essentially possible to create a gallium film on substrates by thermal decomposition of gallium nitride. Unfortunately, the required process temperatures (at least 873K) are too high for practical application in the field of micro systems.

2.1.3 Electroplating

Electroplating generally is a wide spread technology applied for the production of micro devices. It is a deposition process in which metal ions in a solution are moved by an electric field to coat an electrode. The process uses electrical current to reduce cations of a desired material from a solution and coat an object with a thin or thick layer of the material, such as a metal. Possible metals to plate include Sn, Au, Pt and Cu.
Electroplating of gallium is one of the currently used ways to produce bulk gallium from bauxite ore (Dorin, et al., 1988). In addition, publications can be found that describe gallium electroplating in combination with indium as thin film, mainly for special solar cell structures (Aksu, et al., 2007). According to the literature, the gallium cations are obtained by solving a gallium salt in water-based solvent. Usable gallium salts include sulfate, sulfamate and chloride (Zank, et al., 1996), (Andreoli, et al., 1995). A rather uncommon way is also the use of ionic liquid. This is now just being explored for aluminium electroplating.

From the possible gallium salts, gallium(III)chloride has been selected, mainly because it is possible to acquire as commercial product. Gallium sulfate and gallium sulfamate are not easily available, whereas ionic liquid electrolyte-based electroplating is not yet a mature technology. It should be mentioned that the choice also has its drawbacks. Gallium chloride-based electrolyte is alkaline; for example, potassium hydroxide or sodium hydroxide is necessary. Therefore, many materials are damaged in the electrolyte including several metals, and even silicon. However, because the electrolyte is not heated, the attack to silicon is low.
The electroplating solution used for the deposition comprises gallium chloride, and potassium hydroxide. Glycine can be added as complex builder; however, experiments did not show a large influence on the electroplating process. The composition can be found in Table 2. In addition, the mixing of $GaCl_3$ in diluted KOH has to be done very cautiously, because gallium chloride reacts exothermic with water by generating dangerous HCl vapour. Therefore, the mixing should only be done in safe environment, e.g. inside a glovebox filled with N_2 or Ar, or in a chemical draft. It should be noted that the natural air humidity is already enough for the exothermic reaction that starts as soon as the ampoule that contains the $GaCl_3$ is opened.

Table 2. Composition of electrolyte used for gallium deposition

material	content
gallium chloride	1.1mol/l
potassium hydroxide	0.8mol/l
(glycine)	(0.5mol/l)

The purpose of gallium chloride is to provide the gallium ions, whereas the potassium hydroxide dissolving the gallium chloride as well as supplying anions and cations. Glycine can work as a complexing agent that prevents the formation of gallium oxide in the electrolyte.
With the given concentration, the pH value is about 11.
The deposition has been carried out in an electroplating setup that comprises a container made from polymer, a platinum covered titanium electrode, as well as a calomel reference electrode. (Figure 4) The deposition itself can be done at room temperature, no elevated temperature is necessary.

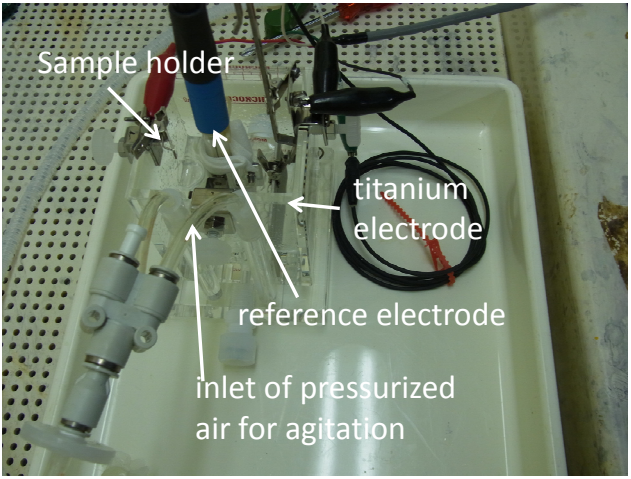
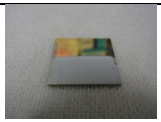
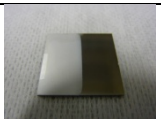
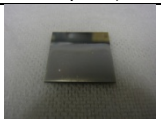


Figure 4. Setup used for electroplating of gallium

Important part of successful deposition is the choice of the correct seed layer. Because the electrolyte solution is alkaline, care must be taken when using metals like copper or titanium. Five different metals have been tested: gold, chromium, platinum, copper and titanium. For the basic test, all layers were sputtered as 50nm thick layers on silicon dioxide covered silicon samples. In case of gold, platinum and copper a 20nm thick adhesion layer of titanium was used additionally. With all metals but titanium, deposition was essentially possible. The titanium seed layer did not survive long enough in the

electrolyte due to its alkaline nature. The qualitative results of the other metals are listed in Table 3.

Table 3. Comparison of different seed layers for gallium electroplating by chloride-based electrolyte

	gold	platinum	chromium	copper
deposition possible	O	O	O	O
quality of deposited layer	O	O	- (wetting is very bad)	O
picture				

The deposition results have been best on gold, platinum and copper. In case of copper, no surface treatment was needed to remove copper oxide prior to the electroplating. Obviously, the electrolyte itself etched it away. For further experiments, it was decided to use gold as seed layer.

To understand the characteristics of the mixed electrolyte the relation of current density and electro potential has been measured by using a potentiostat. Such equipment is able to drive a current controlled by the electro potential measured against a reference electrode. The electro potential is typically adjusted starting from zero until a certain set point and subsequently brought back to zero. The behaviour of the current during such cycle contains valuable information. The current is normalised to the deposition area to allow comparing different sample sizes.

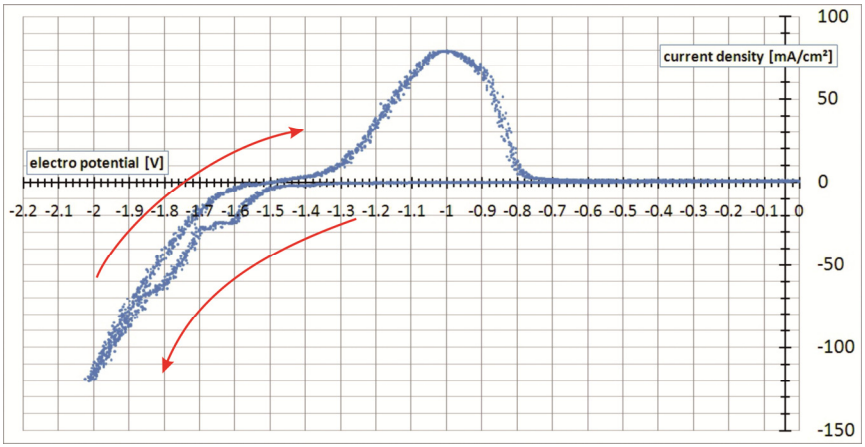


Figure 5. Current density vs. electro potential of the selected chloride-based gallium electrolyte at room temperature, red arrows indicate the time sequence of measurement.

From Figure 5 it can be seen that current flow starts at -1.38V. This is the onset of gallium deposition. At the range between -1.6V and -1.7V a plateau in current density is visible. This is preferred control point for deposition. Different to the characterisation of the electrolyte the deposition is done in current controlled mode. Because the deposition rate is dependent on current, in this mode a chosen value of current is set by controlling the potential. Therefore, a working point that has a small change of current in relation to potential change is advantageous. The current density that matches this plateau equals about 25mA/cm².

Other parameter that is of major interest is the deposition rate. To investigate the deposition rate identical samples have been covered by gallium in a fixed time and different current densities. The height of the deposited gallium was subsequently checked by optical interferometer. For all these samples, a seed layer of Ti/Au with 20nm and 50nm thickness respectively was used. Deposition was done at room temperature.

Although great care has been taken not to exceed the melting point of gallium (30°C) during deposition and subsequent handling, the deposited samples always looked like in liquid state. By scratching, it could be shown that the gallium layer indeed appeared liquid, even the sample temperature is below its melting point. This becomes also clearly visible by deposition of layers with several µm thickness. In such case, the gallium starts to form drop-like structures. (Figure 6) This can be explained by surface tension of a liquid.

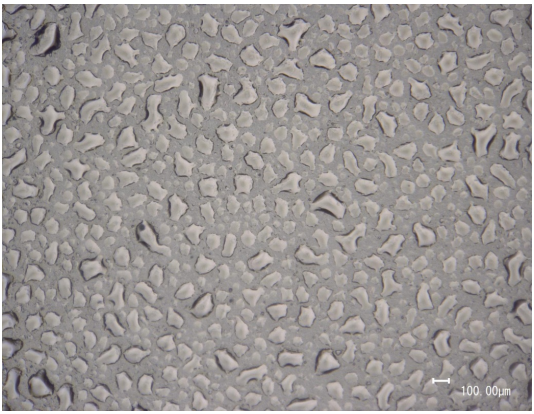


Figure 6. Gallium electroplated forming small droplets due to surface tension showing its liquid structure

An explanation for this phenomenon can be found in existing literature. According to (Skripov, et al., 1988), high purity gallium can exist as a metastable liquid far below its melting point. It can be supercooled. This has also been encountered for evaporated gallium. In experiments by Berwian, it was needed to cool down the sample during deposition below -160°C to prevent drop formation on the surface. (Berwian, 2005) The

extent to which this is a disadvantage during the structuring of gallium should be investigated.

2.2 Lithography

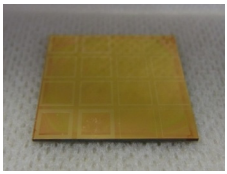
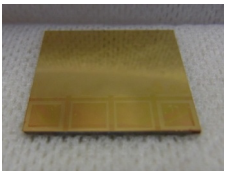
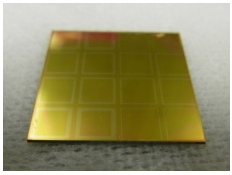
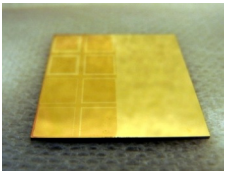
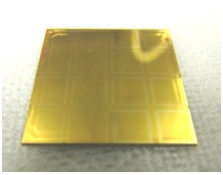
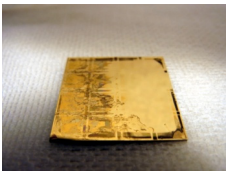
Beside the deposition of gallium, it also needs to be structured to be of use. Since the intended application is the formation of bond frames for encapsulation of micro devices, the ability of forming micro-structures is mandatory. As the gallium is either already liquid, or will become liquid from temperatures above 30°C at latest, any process step that involves temperature treatment should be avoided. In micro technology many methods for patterning of thin films exist, for example wet chemical etching, plasma assisted etching and lift off. They all require photolithography to transfer the desired pattern to the thin film. The used photo resists require various pre and post bake steps to remove organic solvent, facilitate adhesion and chemical stability. The temperature of these bake steps typically is in the range of 60°C to 140°C. Because the viscosity of gallium decreased significantly at elevated temperatures, it seems too difficult to apply photolithography on the deposited thin film. Therefore, lithography after gallium deposition has not been considered.
The alternative is to create an already patterned resist layer on top of an unstructured seed layer before electroplating. When using this technique only the area of the seed layer that is not covered by resist is coated during electroplating process. Therefore, there is no need to etch the electroplated material.
In most cases, electroplated layers are structured by a technique called electroforming. The resist is essentially having the function of a mould, as deposition of the metal will only happen on the areas of the seed layer that are not covered by resist. The empty spaces in the resist are filled by the deposited material. This technique has several advantages. In contrast to subtractive processes, like etching, material is not wasted, since it is deposited only in the needed areas in the first place. This is especially advantageous in case of noble metals, e.g. gold. The second large advantage is the easy formation of thick structures with high aspect ratios. (Kohlmeier, et al., 2002)

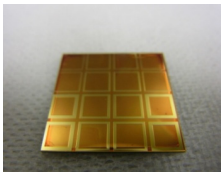
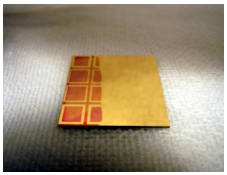
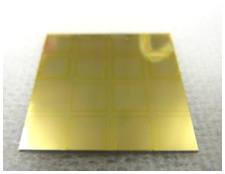
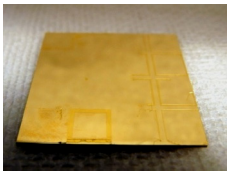
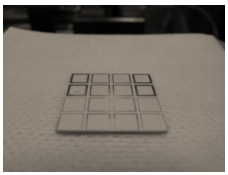
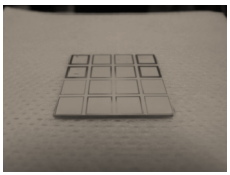
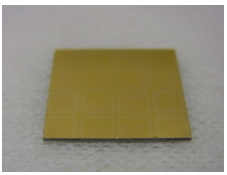
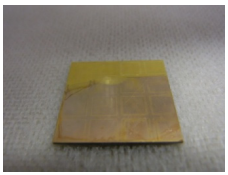
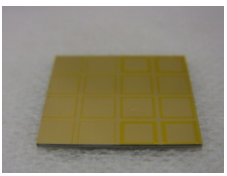
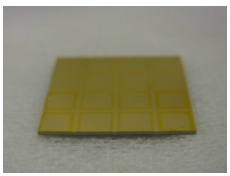
2.2.1 Resist

Electroplating with photo resist masks requires a chemically stable resist with a superior adhesion to the substrate. In case of thick layers, steep sidewalls are also required. Since the desired gallium thickness is relatively thin in this case at about 1µm, which is much smaller than typical bond frame width (~100µm – 200µm), the side wall angle is not so important. It is important to avoid underplating (deposition under the resist) and resistance against attack by the electrolyte.
However, aqueous alkaline solutions attack a non-cross-linked positive resist mask when the pH value significantly exceeds 10. Of course, the stability depends also on the time in

the electrolyte and its temperature. Moreover, one has to consider that the local pH value near the metal deposition can be quite different from the value measured in the electrolyte. The alkaline stability of the resist film can be improved via a hardbake applied at temperatures > 140°C where the resin starts to cross-link. However, such temperatures are beyond the softening point of positive resists, which will make the resist profile worse. Cross-linking negative resists generally show higher resistance to alkaline electrolytes. In case of cross-linked negative resists, hardbake can be applied without the danger of resist softening. However, towards higher hardbake temperatures (= increasing degree of cross-linking), the wet chemical removability of the resist after electroplating decreases. Resist swelling during electroplating in combination with a suboptimum resist adhesion often consequently causes peeling of the resist. In this case, it is important to find a photo sensitive resist that is chemically resistant against the electrolyte because it has to sustain the severe electroplating conditions; indeed, this is particularly difficult for the alkaline-based electrolyte. Therefore, several industrial applicable photo resists have been tested under electroplating conditions with the selected highly alkaline electrolyte by putting samples coated with the different resists into the electrolyte and observing the reaction over time.

Table 4. Results of experiments to determine the chemical resistance of different resists in gallium electroplating solution

resist name	**before exposing to electrolyte**	**after exposing to electrolyte**	**failure mode**
OFPR 800			 immediate dissolving of resist
TSMR-V90			 immediate dissolving of resist
PMER P-LA 900			 after ca. 3.5 min dissolving of resist

resist name	before exposing to electrolyte	after exposing to electrolyte	failure mode
AZP4620			 immediate dissolving of resist
PMGI/ OMR 83			 after ca. 5 min resist is partly lifted and removed
ProTEK			 no change
PMGI/ AZP4620			 resist dissolves in <1 min
OMR83			 no change

It has been found that as expected only negative resists can endure the severe conditions long enough to be further considered further (Table 4). Samples coated with the negative resists OMR83 and ProTEK have been used for further experiments, including real electroplating of gallium to confirm its function during the real process. Surprisingly ProTEK resist started to immediately delaminate from the sample surface after application of an electrical field. It was tried to improve the adhesion by high temperature treatment of the sample (700°C, 30min, N_2) to remove water and hydroxyl groups on the surface as well as hard bake (145°C, 30min). It was not possible to solve this adhesion problem. The

fact the resist starts to peel off as soon as the electrical field is applied although it can withstand the highly alkaline solution up to several hours (it was developed as etch mask for KOH etching of silicon) implies an unusual peeling mechanism. Gallium electroplating is done at high electro negativity. For this reason, it is essentially very difficult to avoid the codeposition of hydrogen on the sample surface. It is suspected that this (elemental) hydrogen is attacking the resist layer itself or its adhesion layer, called PSB primer, and leads to the immediate resist removal. The resist that showed the most promising behaviour is OMR83 from Tokyo Ohka Kogyo Co.
After the basic applicability of OMR83 resist has been proved by experiment the detailed process parameters and conditions needed to be found and optimised. Not optimised resist shows severe underplating. (Figure 7)

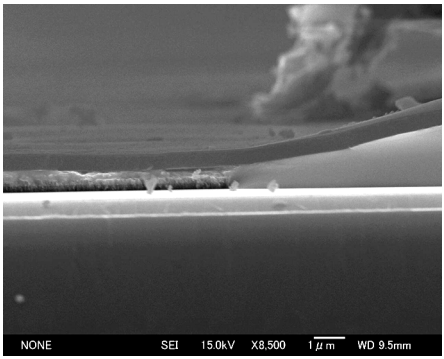


Figure 7. SEM cross section of sample after gallium electroplating showing severe underplating (right side if picture) of OMR83 resist due to the non-optimised condition of resist coating.

To prevent underplating optimisation of deposition parameters was needed. This optimisation work concentrated on the stability of the resist. Exposure and development conditions have been kept stable.

Table 5: Experimental condition and result to test the influence of annealing before resist deposition. O = succeed, X = failed, Δ = unstable (sometimes succeed, sometimes failed). Condition for success is the ability of the resist to remain stable up to 10min during electroplating without underplating.

		annealing time before resist deposition (with post bake (145°C, 20min)			**annealing time before resist deposition (without post bake (145°C, 20min)**		
		5min	10min	15min	5min	10min	15min
temperature	110°C	X	X	X	X	X	X
	200°C	X	X	X	X	X	X
	250°C	X	X	Δ	X	X	X
	350°C	X	X	O	X	X	X
	400°C	X	O	O	X	X	X

As can be seen from Table 5 post bake is mandatory, as well as a temperature treatment of the sample surface before resist coating. This temperature treatment should be at least 350°C. After the optimisation the resist exhibits enough stability to be used. Experimental results show that this resist can survive typically up to 10min. Whereas this sounds like a short time, given the deposition rate, as well as the need to deposit layers up to only about 1µm thickness, it is enough.

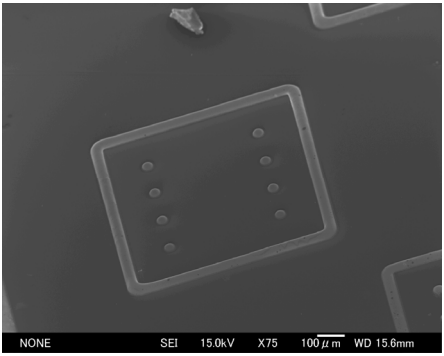


Figure 8. Gallium structure (50µm wide bond frame with electrical contacts) electroplated inside negative resist without underplating after resist deposition parameter optimisation.

Table 6 shows the used process condition of the OMR83. It should be noted that the hard bake at 145°C as well as the initial annealing of 400°C is essential. In Figure 8 gallium electroplated in resist deposited with optimized parameters is shown.

Table 6. Process parameters of OMR83 resist withstanding electroplating conditions of gallium

no.	process step	parameter
1	annealing of silicon sample	400°C, 10 min
2	spin coating of OMR83, 60cp	5000 rpm, 20 s
3	pre-bake	90°C, 20 min
4	exposure	100mJ/cm²
5	development	OMR developer, 80s
6	post bake	145°C, 20 min

2.2.2 Resist removal

As previously mentioned, high chemical stability of the photo resist is desired during electroplating. By contrast, after gallium deposition, an easy removal of the resist mask is necessary. The typical process for resist removal is either wet chemical treatment or oxygen plasma ashing. In the latter case the substrate is heated by the plasma impact, furthermore oxidation of the surface is facilitated. Therefore, it is not suitable for the resist removal in this case. In case of wet chemical treatment, a resist stripper fitting to the resist

is usually applied at a higher temperature between 80°C – 120°C for several minutes. Such a treatment is able to remove even cross-linked negative resist after some time. Due to the existence of gallium metallisation increasing the temperature is not desirable to prevent flowing of liquid metal by reducing its viscosity. Therefore, it is necessary to find a way to remove the resist that has been used during electroplating to structure the gallium by a stripping process at room temperature. Only applying resist stripper at room temperature did not yield satisfying results. Even after 24h, some resist still remained on the wafer surface. (Figure 9) By applying ultrasonic support, the result entirely changes. When putting the wafer in resist stripper and continuously agitating ultrasound, all resist could be successfully removed in all cases after 7h treatment at the latest. (Figure 10)

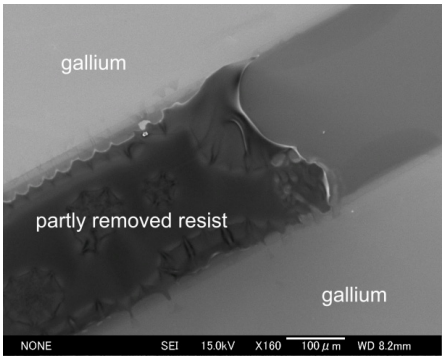


Figure 9. SEM top view of structure after gallium electroplating and resist stripping at room temperature without ultrasonic support. The resist is only partly removed.

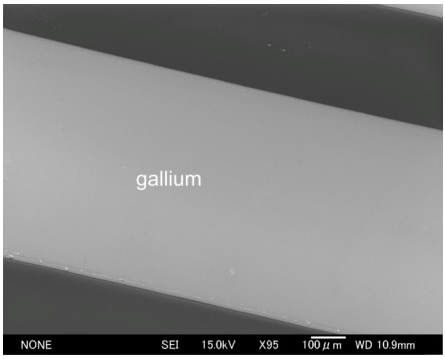


Figure 10. SEM top view of structure after gallium electroplating and resist stripping at room temperature with ultrasonic support. The resist is entirely removed.

The stripper that was applied successfully in this way is 502A from Tokyo Ohka Kogyo Co. Treatment for 7h seems long and thus expensive, although since such wet chemical stripping process can be done as a batch process, the costs can still be low enough. There is a possibility that the ultrasonic agitation leads to a local increase of temperature, although it was observed that in all samples gallium did not start to flow on the seed layer, even after the resist was removed.
Another method to remove the resist could be the use of a sacrificial layer underneath the resist that is etched away after electroplating. Unfortunately, much like aluminium, gallium has a poor chemical stability in most used etchants.

2.2.3 Seed layer removal

Beside the resist deposition and stripping, the subsequent removal of the seed layer also holds strong importance. Especially in the case of application for vertical electrical

contacts, electrical shortcut between the different gallium bonding areas must not be accepted.
The seed layer comprises several 10nm Cr and several 10nm Au (typical values: 10nm Cr and 50nm Au). Both layers gold and chromium needs to be removed. ICP etching processes have not been considered due to the plasma induced temperature increase of the wafers during the process. Wet etching of gold is usually being done by I2 : KI : H2O solution. Etching experiments done showed no measureable etching attack of gallium by this etchant. It can be considered that the selectivity between gold and gallium is very high and entirely no problem during the seed layer removal occurs. In case of chromium etching, the situation is different.

Table 7: Selectivity gallium : chromium of certain typical chromium etchants as measured by experiments.

etchant	**etch selectivity between gallium and chromium**
HClO4 : H2O : (NH4)2Ce(NO3)6 20 : 5 : 2	>500 : 1
HCl : H2O2 3 : 1	10 - 20 : 1
HCl : H2O : H2O2 3 : 2 : 1	10 - 15 : 1
HCl : C3H8O3 1 : 1	8 - 10 : 1
KMnO4 : NaOH : H2O 2 : 3 : 12	80 - 100 : 1

The etching rate difference of several chromium etchants has been investigated in several experiments, whereby samples with electrodeposited gallium (1µm thick) have been prepared on 50nm Au / 20nm Cr seed layer. After resist removal and gold etching, the samples have been exposed to the Cr etching solutions. The etching has been performed until either the chromium layer or the gallium layer visibly has been etched away. (Figure 11 and Figure 12) The thickness of the remaining metal has been measured and used to calculate the selectivity. The etching solution was always kept at room temperature for obvious reasons. As can be seen in Table 7 it was found that in all cases gallium was etched much faster than chromium. The best result was achieved by HCl : $C_3H_8O_3$ 1 : 1. After 40s, all chromium (20nm) has been removed, although about 160nm – 200nm gallium has also been etched at the same time. This loss in gallium thickness has to be taken into account during gallium deposition. Therefore, to achieve 1µm layer thickness for bonding, 1.2µm gallium has to be deposited to offset the etching effect during seed layer removal.

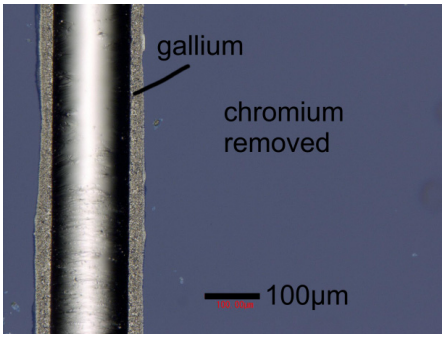


Figure 11. Optical microscope top view of gallium structure after successful seed layer removal.

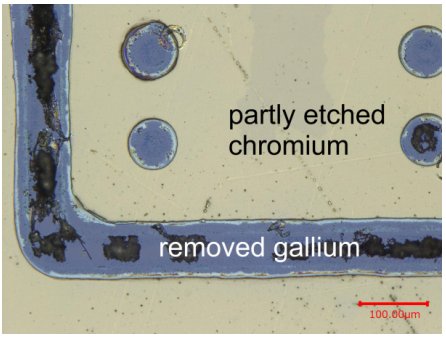


Figure 12. Optical microscope top view of removed gallium structure with remaining chromium seed layer after unsuccessful etching trial of seed layer due to too bad selectivity.

3. Characterization

To obtain a comprehensive understanding of the bonding mechanism and results different complementary characterisation methods have been used. Beside scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDX) methods that allow the analysis of time and temperature dependent development of physical properties of samples are necessary. As such techniques, conductivity measurements as well as shear strength test and hermeticity tests have been applied.

3.1 Mechanical (shear strength)

One of the most important quality parameter of a wafer bond is the mechanical strength of the bond. Characterisation of the bonded interface and the entire device that uses bonding techniques in its production require the determination of the bonding strength itself. Different qualitative methods like dicing test and tape test as well as quantitative methods such as shear test and micro chevron test are being used. Because dicing is a commonly used technique to separate the chips during manufacturing, the dicing test is often used to monitor the bonding strength. Other approaches provide adequate failure criteria and enable the comparison of different bonding technologies and process parameters. There are several defined criteria for the mechanical strength. The most used criteria are fracture toughness and shear strength. (Mueller-Fiedler, et al., 2009) It is possible to measure the first one by micro chevron test and the later one by shear test. In the fields of microelectronics and micro systems technology, the shear test is often used to evaluate the bonding strength of different packages with and without intermediate layer. Because there are no limitations regarding the interface structure, it can be carried out with finished devices as well as special test structures. The shear strength is also a suitable value to characterise bonded structures consisting of materials with different coefficients of thermal expansion. For this investigation, the shear test has been chosen. Essentially any surface geometry of a bonded interlayer can be used with the shear test. In this investigation, the compressive shear test has been used. A commercial test equipment TIRA test 2805 was used. The sample is fixed in a special mounting that allows loading at 45°, see Figure 13.

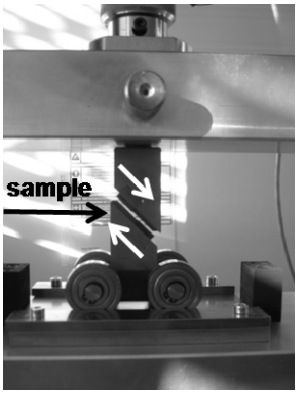


Figure 13. Mounting of shear test sample at 45°

Under the condition of such mounting, the shear strength τ_{schub} can be calculated by:

$$\tau_{schub} = \frac{F_{\max} \times \sin(45°)}{A_{bond}} \quad (7)$$

F_{max} is the maximum force achieved during testing and A_{bond} is the tested bond area. (Vogel, et al., 2012)
During the shear test, the sample is elastically and plastically deformed until its failure, displacement (deformation) and force are logged. The maximum force is obtained from the point of failure. Figure 14 shows a sample shear test measurement.

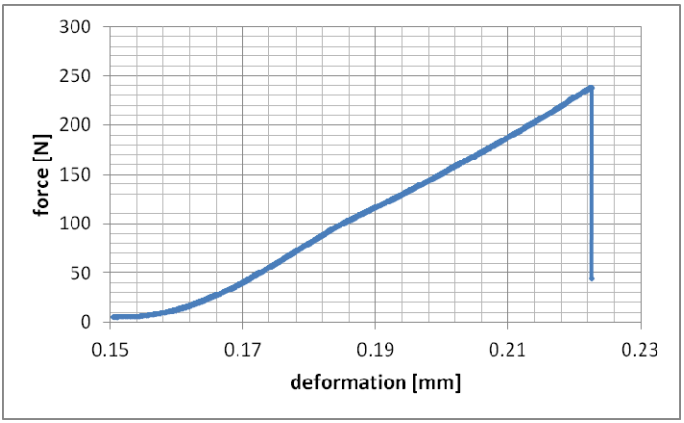


Figure 14. Example for displacement/force measurement results of shear test of a bonded sample

3.2 Electrical (conductivity)

The measurement of electric conductivity is a useful supplement of other techniques. Because the electric conductivity of an interface depends on its composition this method can be used to analyse changes in interface composition depended on time and temperature. Furthermore bonding of vertical electric contacts is of basic interest in case of hetero integration and 3D stacking of devices such as shown in Figure 15. For such integrated circuits electrical signal lines must be connected vertically during bonding between the two substrates (typically a via structure is connected to a sensor or actuator).

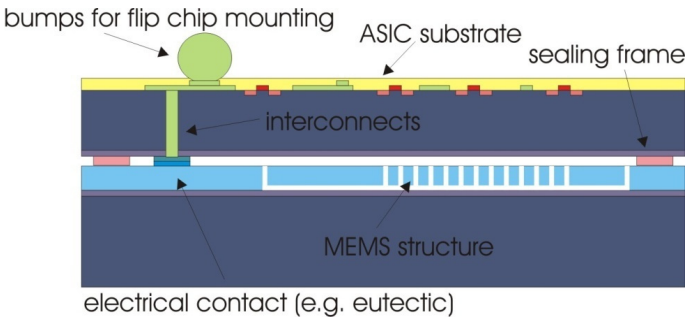


Figure 15. Schematic cross section of a typical 3D integrated MEMS structure showing the need for vertical interconnect.

Because the electrical resistance of the bonding interlayer at the vertical interconnect will have an impact to the contact resistance of the entire via structure it is important to investigate it. Most applications require a low resistance of the electrical contacts. To measure the electrical conductivity of such vertical contacts a simple structure that allows electrical 4-wire measurement has been designed and fabricated. (Figure 16) 4-wire measurement is a traditional measuring method to measure a resistance. As shown in Figure 17, it minimises or eliminates the effects of lead resistance by measuring the voltage across the resistor under test with a second set of test leads. Due to the high input impedance of the voltmeter, the current through the sense leads is negligible, and the measured voltage is essentially the same as the voltage across the resistor under test (Keithley Instruments, Inc., 2002). The test structure comprises a line with two consecutive vertical contacts that are bonded and contact pads for contacting during the measurement.

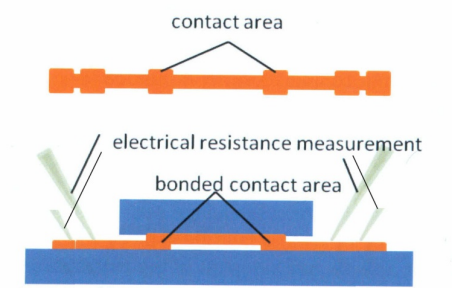


Figure 16. Schematic image of the test structure to observe the vertical resistance of bonded contacts

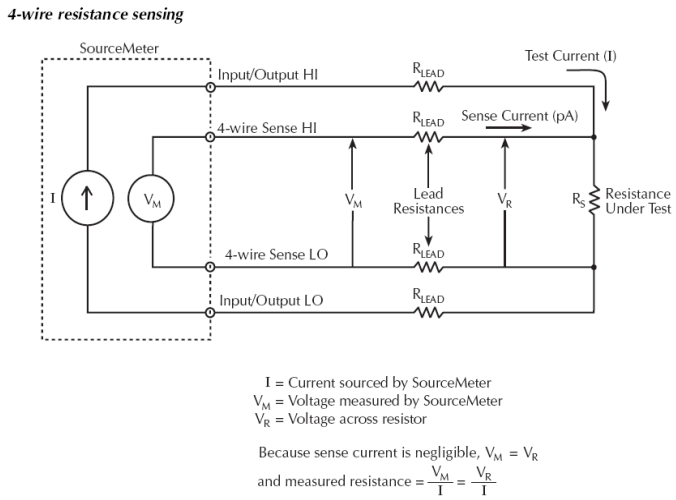


Figure 17. Schematic figure of 4-wire resistance measurement (Keithley Instruments, Inc., 2002)

3.3 Hermeticity testing

For various MEMS applications precise control of their in package atmosphere is necessary. This includes absolute pressure sensors, micro switches, accelerometers and gyroscopes. To make matters more complicated such devices need to interact with their environment by via interconnects and coplanar access for example. To ensure reliability a strong need to develop testing methods of these tiny and particular hermetic packages arises. Besides the helium leak detection method, which is frequently used for testing microelectronic packages, a number of techniques fitting the special needs and requirements of micro mechanical devices have been developed and applied within recent decades. One of the challenges is the comparable small inner volume of the current days MEMS.

3.3.1 Membrane deflection

Optical detection of membrane deflection is another possibility of leak rate measurement. In wafer level packages, a cap that contains a cavity is bonded to a substrate. After bonding, if the package is at least quasi-hermetic, the pressure inside differs from the outside environment pressure. In case the pressure is lower inside the cavity than outside the membrane is bended inwards. If the pressure difference is null, than there is no membrane deflection. By knowing the correlation between the membrane deflection and

the pressure difference, it is possible to obtain pressure change over time. This can be done either by observing the pressure difference over a long time or by bombing the package with gas similar to the helium leak test. The measurement of the membrane deflection is being done preferably by optical profilometer. A mechanical profilometer may influence the deflection during measurement; a white light interferometer is well suited, for example. It usually has a large optical measurement range as well as nanometer scale resolution.

The relation between the membrane deflection and pressure difference can be obtained by FEM simulation and analytical calculation. In the following, the analytical model will be described. For an isotropic clamped square shape membrane, the differential pressure P_{diff} is given by (Bonnotte, et al., 1995):

$$P_{diff} = C_1 \frac{t_m \times h}{a^2}\sigma + C_2 \frac{t_m \times h^3}{a^4}\frac{E}{1-\upsilon} + C_3 \frac{t_m^3 \times h}{a^4}\frac{E}{1-\upsilon^2} \quad (8)$$

h is the central membrane deflection, a is the half length of the membrane at the edge and t_m is the thickness of the membrane. E and υ are the Young's modulus and Poison ratio respectively; δ is the residual membrane stress. C_1, C_2, and C_3 depend on the membrane shape. For square membranes there are: C_1 = 3.4075, C_2 = 1.84 and C_3 = 4.129 (Lellouchi et al. 2010). In case of low deflections and low residual stress term 1 and term 3 dominate (Bosseboeuf, et al., 2006). For this reason, the second term is omitted and can be disregarded in this case. When using the measurement over time approach, where a cavity is sealed under lower pressure and the decreasing of the membrane deflection is measured over time, the leak rate L of a package can be calculated by:

$$L = \frac{\Delta P_{diff}}{\Delta t \times V} \quad (9)$$

Δt is the time difference in between measurements and V is the inner volume of the package.

By combining formula 8 and 9, the leak rate equals:

$$L = \frac{\Delta h\left(C_1 \frac{t_m \times h}{a^2}\sigma + C_3 \frac{t_m^3 \times h}{a^4}\frac{E}{1-\upsilon^2}\right)}{\Delta t \times V} \quad (10)$$

With this formula, it is possible to directly calculate the leak rate by membrane method.

3.3.2 Test by resonating MEMS structures

The quality factor and the bandwidth of an oscillating system depend on the damping, which occurs from the surrounding gas. The damping is a function of the density (pressure) of the gas. If all the dependences are known it is possible to calculate the pressure of the surrounding gas of a resonant structure from the quality factor and bandwidth. Resonant structures are well known in MEMS fabrication, for example gyroscopes. Such sensors need a very low pressure at around 100Pa and lower to work properly. The knowledge to fabricate and design these devices can be used to create dedicated resonant pressure sensors (Parridge, et al., 2005). Starting from analytical computations to calculate the dependence of quality factor and pressure of a micro structure a design is developed as FEM model and consequently simulated until it meets target conditions (pressure range). The damping simulation is based upon the squeeze film theory (Mehner, et al., 1998) and the analytical approximated vacuum pressure dependency of the viscosity (Veijola, et al., 1995).

$$Q = \frac{m\,\omega_0}{\beta} \tag{11}$$

The quality factor (11) of a resonating micro system depends on the mass m, the eigenfrequency ω_0 and the mechanical impedance β of the system. The mechanical impedance of a system where the damping is of squeeze film type between parallel plates depends on the geometry (a,b are the plate dimensions, d is distance between plates) and the effective viscosity η_{eff} of the surrounding gas.

$$\beta = \frac{\eta_{eff}\,a^3 b}{d^3} \tag{12}$$

The ambient pressure p_a is responsible for the change of the viscosity η, leading to the effective viscosity. η_0 is the viscosity at pressure p_0 and λ is the mean free path of the gas molecules. Kn is the so called Knudsen number.

$$\eta_{eff} = \frac{\eta_0}{1 + 9.64\underbrace{\left(\frac{\lambda}{d}\frac{p_0}{p_a}\right)^{1.16}}_{Kn}} \tag{13}$$

The upper end of the measurement range is determined by the beginning viscous flow of ambient gas combined with low variations of its dynamic viscosity. The lower end of the measurement range is determined by the ratio between gas damping and the sum of all other damping effects (e.g. thermoelastic internal friction, mounting loss, damping by electrical feedback). Figure 18 shows the design of a typical resonant structure.

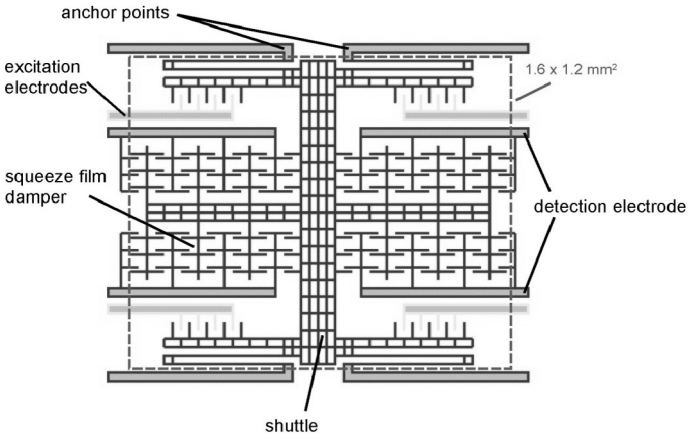


Figure 18. Typical design scheme of a resonant MEMS structure used for hermeticity testing

Such resonant structures can be fabricated with the same technologies like functional MEMS devices, for example with Bonding and Deep Reactive Ion Etching (BDRIE) technology (Hiller, et al., 2005). It was found, that resonant structures prepared with such technique show an almost linear behaviour between pressure and quality factor on a double logarithmic scale between 0.1Pa and 1000Pa. This makes it suitable for a wide range of applications. The measurements taken indicate that it is possible to achieve accuracy below 5%. (Froemel, et al., 2006)

3.3.3 Test by FT-IR spectroscopy

The FT-IR spectroscopy represents a non-destructive method for hermeticity characterisation of bonded micro-structures. The property of gases to absorb radiation with a specific wavelength allows its explicit characterisation (Veyriéa, et al., 2005). Therefore, when a package is exposed to a tracer gas atmosphere and the gas is able to leak into the structure it can be detected via the specimen's transmission spectra. Therefore a gas with an absorbance between k=9100 cm-1 to k=2000 cm-1 in the case of silicon substrate material has to be used. Due to its double absorbance peak at k=2240 cm-1 and k=2210 cm-1, its inert chemical behaviour and the ability to be distinguished from atmospheric gases, nitrous oxide (N_2O) is used. The assessment procedure comprises the

recording of the transmission spectra of the specimen filled with ambient air (T_{ref}), the bombing with the tracer gas for three hours at a pressure of 500 kPa and the repeated transmission spectra (T_{N2O}) recording subsequently. The time between end of bombing and begin of measurement has to be kept as short as possible to prevent N_2O leaking out of the cavity. Such already leaked gas amount cannot be defined, which results in an incorrect calculated leakage value. By the calculation of the transmission ratio (T_{N2O} / T_{ref}) for k=2240 cm-1, the knowledge of the cavity's depth (d), the temperature during measuring (Θ) and the extinction coefficient a the internal nitrous oxide pressure (p_{N2O}) can be determined by using the Beer-Lambert Law and the ideal gas law (R = Boltzmann constant).

$$p_{N2O} = \frac{-\log\left(\frac{T_{N2O}}{T_{ref}}\right) \times R \times \Theta}{d \times a} \qquad 14$$

The leakage detection by FT-IR spectroscopy allows the hermeticity characterisation of encapsulated micro-structures by the verification of penetrated tracer gas. The test is very fast, more comfortable than the helium leak test and has a better signal-to-noise ratio due to the absence of N_2O to ambient atmosphere. Furthermore, the evacuation of the testing chamber is not essentially needed so that the delay before measuring can be reduced. (Froemel, et al., 2011)

3.4 Scanning electron microscopy

To document the morphologic development of bonded and thermal processed samples the scanning electron microscopy (SEM) has been used as imaging technology. With the help of an energy dispersive detector the entire spectrum of all during the scanning process emitted X-ray quanta can be recorded and used for the chemical analysis of the sample (energy dispersive X-ray analysis (EDXA)). In the framework of this dissertation, several different microscopes from JEOL, Hitachi and Zeiss have been used. Acceleration voltage was adjusted up to 20kV and sample current was adjusted to 8nA. The analysis of the recorded EDX spectra was done with proprietary software belonging to the respective EDX detectors. The quantification of the elements was done by the characteristic K and L lines for each element.

Observation of interface morphology requires cross section of the bonded areas. To obtain information on structure and composition these cross sections must be of high quality. In this work ion beam cutting has been used as the main method to prepare samples for SEM

and EDX analysis. In this method, the sample is bombarded perpendicular with one or more argon ion beams. These ion beams remove matter by physical impact; an aperture is used to create a straight cut from the round shape ion beam. The used equipment is a Leica TIC 3X. In significant difference to traditional sample preparation methods, the ion beams are applied in parallel to the interface. Therefore, the material is not polished, but cut straight very cleanly. No prior or subsequent polishing is necessary. The cutting speed does not depend on material hardness, for those reason cross sections of different materials like metals and silicon can be obtained smoothly. No debris or deformation is created. To cut through a bonded wafer pair and open a sufficient part of the interface it takes about 5h at standard conditions.

4. Gallium-based solid liquid interdiffusion bonding

So-called solid liquid interdiffusion bonding (SLID) is a technology that generates bonds that can withstand higher temperatures than the process temperatures. This is being done by alloying at least two different metals. One of the metals has a low melting point T_{ML}, while the other material has a higher melting point T_{MH}. The bonding process takes place at a temperature higher that the melting point of the metal with lower melting temperature. As a first step, the liquid phase will wet the surface of the metal that remains solid. The increased diffusion that takes place from the solid phase into the liquid phase leads to a rapid increase of the high melting point metal inside the liquid phase. After reaching saturation of the solubility intermetallic phases with a higher melting point than the bonding temperature are formed. This goes on until all the liquid phase has been consumed, after which only diffusion in the solid state continues. This diffusion continues until the equilibrium dictated by the phase diagram is reached. The resulting intermetallic phase(s) has (have) a higher melting point than the process temperature. The second metal remains solid during the entire process, hence the name of the process. It has been introduced first by Fairchild Semiconductor (Bernstein, et al., 1966) as a method for semiconductor chip assembly. The systems described in this very first work are Ag-In, Au-In and Cu-In.

One of the significant advantages of SLID is the possibility to bond at low temperature. With this first publication, Bernstein has defined the acronym SLID. Table 8 shows a selction of currently used SLID bonding processes. Beside SLID also the acronym of TLP (Transient Liquid Phase Bonding) is known. TLP is a similar process, albeit with significant differences. First published by Duval, et al. (Pratt & Whitney Aircraft) in 1974, it uses the substrates as one of the components; the low melting point material is applied as interlayer. Due to the very different volumes the interlayer is entirely solved inside the substrate material at the end of the bond resulting in a homogeneous interface. This homogeneous interface has the same or similar fracture toughness as the substrate material (Duvall, et al., 1974). Both processes have in common the isothermal solidification from liquid phase. The bond interface of both processes is very different.

Table 8: Selection of most common used SLID bonding material combinations

material system	TML	TMH	target intermetallic phases	representative publication
Ag-In	197°C	962°C	Ag2In, Ag3In	(Bernstein, et al., 1966)
Au-In	197°C	1064°C	Au7In	(Bernstein, et al., 1966)
Cu-In	197°C	1085°C	Cu7In3 (δ)	(Bernstein, et al., 1966)
Ag-Sn	232°C	962°C	Ag3Sn, ζ	(Chen, et al., 1997)
Au-Sn	232°C	1064°C	Au5Sn	(Lee, et al., 1992)
Cu-Sn	232°C	1085°C	Cu3Sn	(Bartels, et al., 1994)

In case of SLID bonding, the interface comprises intermetallic phase(s), whereas in case of TLP bonding the interface is homogeneous. (MacDonald, et al., 1992) Often this difference is disregarded by authors, concentrating only on the solidification part. The required thickness tA and tB to form the intermetallic phase of AxBy of the two metals A, B can be calculated by:

$$\frac{t_A}{t_B} = \frac{\rho_B \times M_A \times x}{\rho_A \times M_B \times y} \qquad 15$$

In this formula M_A and M_B are the respective molar masses and ρ_A and ρ_B the densities. For all following calculations, the material parameters in Table 9 have been used.

Table 9: material parameter used in this work to calculate layer thickness

material	density	molar mass
Au	19.32g/cm³	196.9665g/mol
Cu	8.92g/cm³	63.546g/mol
Ga	5.904g/cm³	69.723g/mol

4.1 Diffusion

The key mechanism of the SLID bonding is the physical process of diffusion. In this chapter a short introduction to this phenomenon will be given. Fundamental knowledge about this is required as background for the overall work in this thesis.
Nowadays it is elementary knowledge that in a material system with local concentration differences a movement of elements happens with the goal to equalise these concentration differences. This transport of matter is called diffusion. It happens in all kind of material and all states of matter. The person describing the nature of the process first was Adolf Fick. (Fick, 1855) His main findings can be condensed in this form (one-dimensional):

$$J_i = -D_i \frac{\partial c_i}{\partial x} \qquad 16$$

J_i is the number of atoms or moles of element i that move per time unit (seconds) through a given area (m²) in x-direction. This particle current is proportional to the difference on concentration c. The diffusion coefficient D is the characteristic factor of a diffusion system. This formula is known as 1st law of Fick. As the name implies, it is not the only law of Fick. Formula 16 is valid in systems with constant concentration difference, whereby

such systems can typically by liquid or fluid. For solid systems, the concentration usually at least locally changes with time. For these cases, the 2nd Fick law is used:

$$\frac{\partial c_i}{\partial t} = \frac{\partial}{\partial x}\left(D_i \frac{\partial c_i}{\partial x} \right) \qquad 17$$

In case the diffusion coefficient remains constant and is independent on location and concentration, it changes to:

$$\frac{\partial c_i}{\partial t} = D_i \frac{\partial^2 c_i}{\partial x^2} \qquad 18$$

Is there existent a spatial distribution of concentration and thus the particle flow is not limited in one direction it follows

$$\frac{\partial c_i}{\partial t} = D_x \frac{\partial^2 c_i}{\partial x^2} + D_y \frac{\partial^2 c_i}{\partial y^2} + D_z \frac{\partial^2 c_i}{\partial z^2} \qquad 19$$

In crystalline solid metals, diffusion physically occurs by defects inside the crystal lattice. These defects can be point defects, line defects or area defects. For point defects, vacancies are very important. In addition, interstitial atoms, especially foreign atoms, play an important role. Line defects are responsible for diffusion in dislocations. Area defects are the background of diffusion at grain and phase boundaries. The thermodynamic necessity for the existence of vacancies follows the effect of lowering the free enthalpy of the metal lattice. The equilibrium concentration of vacancies and interstitial atoms can be calculated. For the regarding physical background extensive literature exists, e.g. (Simmons, et al., 1960). Metal usually contains dislocations and grain boundaries. In an edge dislocation, for example an additional lattice plane is inserted. Above the dislocation line, the atoms have some smaller distance than below. It is reasonable than in the area of lower atom concentration movement of atoms is easier. Regarding theory, behaviour and properties of dislocations it is referred to literature. (Cottrell, 1953) In comparison to dislocations in the area of grain boundaries, the crystal lattice is much more disturbed. The so-called high angle grain boundaries have a highly disturbed order. Small angle grain boundaries are characterised by the smallest disturbance. They essentially comprise edge dislocations.

Whereas diffusion is happening even in single element materials (self diffusion), in SLID at least two different elements are participating. In such a case, the diffusion can be characterised by the interdiffusion coefficient $\widetilde{D}$.

With the diffusion coefficients D_A and D_B of the elements A and B with the molar fraction N_A and N_B, it is defined by

$$\widetilde{D} = N_A D_B + N_B D_A \qquad 20$$

This has been first derived by Darken. (Darken, 1948)

4.2 Background and history

The ability of two or more metals to form an alloy, at a temperature above the melting point of one of the metals, whereas the alloy has a melting point higher than the one of the original metals has already long been used without naming it SLID or TLP. (MacDonald, et al., 1992) For example, to repair the damage of teeth, a material was needed that is workable at body temperature yet soon becomes solid and strong. For this purpose, mercury that is liquid at room temperature has been mixed with copper powder, for example. The resulting paste is called amalgam (Smith, et al., 1956). The amalgam has been applied to the broken teeth and formed in the desired shape. Copper (usually from coins) was ground to fine powder and mixed just before putting it in the tooth. When the alloying was completed, the amalgam became solid and durable. This material has been applied over many decades. When it has become known and accepted that mercury is dangerous for human health, substitute materials have been researched. The most promising candidate was gallium due to its melting point of 30°C. At the beginning, such gallium amalgams did not exhibit satisfactory mechanical properties (Pinascoa, et al., 2001). Especially the volume expansion during hardening proved a significant problem. Although the properties could be significantly improved with intensive research, the gallium amalgam never saw extensive use. This is because meanwhile UV-curable ceramic pastes emerged that are mainly used nowadays, given that they are durable and can be adjusted to the teeth colour. Outside of dentistry, amalgams have also been used as a bonding material for constructing in mechanical engineering. (Freedmann, et al., 1974)
Beside this pure application-driven activity, gallium and the formation of its alloys have also been extensively investigated from a scientific perspective. (Wilkinson, 1948)

Since about 20 years for application in the field of microelectronics first investigations to use such amalgams has been carried out. The possibility to substitute lead-based solders was one of the driving factors behind such a development. MacKay (MacKay, 1993) intensively researched Ga/Ni, Ga/Ni/Cu, Ga/Cu, Ga/Ag/Cu amalgams and their properties. As a potential application, he suggested die attachment, flip chip bonding, heat sink attachment and via filling, among others. He showed that the properties of such amalgams are very promising for the mentioned applications. Baldwin from Lucent Technologies Inc. (Baldwin, et al., 2000), (Baldwin, et al., 1997) described the use of Ga/Cu/Ni amalgam for flip chip bonding in detail. For such flip chip bonding, the amalgam would be screen

printed on bare silicon chips and subsequently bonded to FR4 substrates with stencil printed Pb/Sb solder bumps. According to their results, the flip chip bonding yielded satisfactory results whereas some problems remained. For example, the shelf life of the amalgam paste used for screen printing is only some hours until it hardens. Bhattacharya demonstrated the application for via filling (Bhattacharya, et al., 2000). The premixed paste was screen printed into vias and subsequently cured at 130°C for 16 hours to allow complete alloying.
Gallium amalgams have meanwhile also entered the field of MEMS devices. Intel has filed a patent to use such amalgams as a bonding material to hermetically seal MEMS devices (Lu, et al., 2006). They also apply the paste by screen printing in a very comparable way like glass frit material is used for bonding in the field of MEMS packaging.
Although the use of amalgams has been successfully demonstrated, they have not yet found their way into industrial application. The reason is the very limited shelf life as soon as it is mixed. To overcome this shortcoming, the gallium layer should be formed separately from the bonding partner material. In the following chapters, the bonding with such a setup is described.

4.3 Gallium – gold SLID bond process

The system gold-gallium is the strait forward idea to implement wafer level bonding based upon the alloying of gallium with a metal. Gold does not have a stable oxide that could prevent or hamper necessary diffusion processes. In the following part, the theoretical background, experiments and the results of gold-gallium bonding are described, followed by a discussion and comparison of all results at the end of the chapter.

4.3.1 Theory

The Au-Ga system has been investigated intensively in the past (Simic, et al., 1976). The binary alloy phase diagram shows that several intermetallic phases have been identified. (Figure 19) The phase diagram implies that it is possible to form alloys near room temperature that have a high melting point, $AuGa_2$ for example has a melting point of 491°C. Such low reaction temperature would be very useful as it essentially allows room temperature bonding of devices. The melting or decomposition points of all possible intermetallic phases are higher than 200°C.

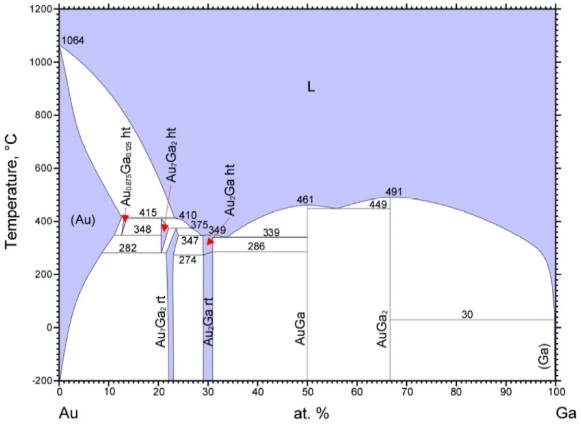


Figure 19: Binary alloy phase diagram of Au-Ga (Massalski, et al., 2006)

The alloying of gold and gallium is not uncommon in the field of jewellery. To make necklace, rings or other jewellery more attractive and appealing it is common to change the colour of noble metals like gold by alloying it with other metals. Accordingly, $AuAl_2$ is known as “purple gold” due to its colour, whereas $AuGa_2$ has a light blue colour and thus is called “blue gold”. (Figure 20) From this application, it is also known that $AuGa_2$ is brittle and has low mechanical strength. (Fischer-Buehner, et al., 2010) For this reason, other phases with higher gold content should be preferred for wafer bonding.

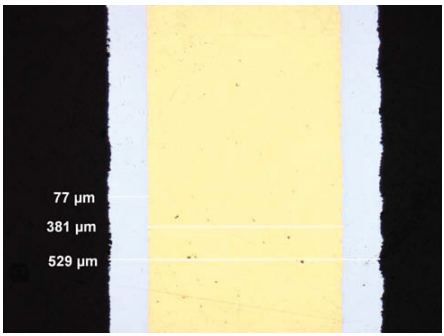
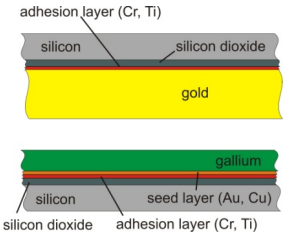
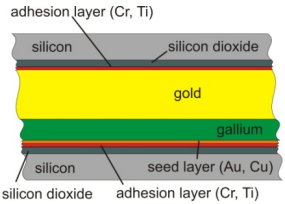
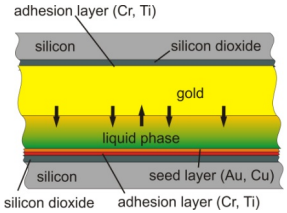
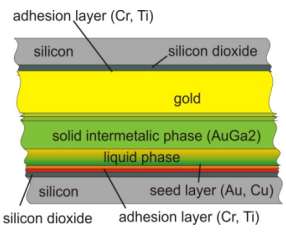
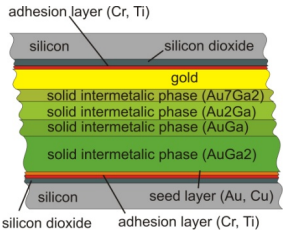
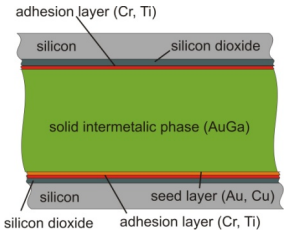


Figure 20. Blue gold layer of AuGa2 on fine gold after dip-coating for jewellery (Klotz, 2010)

The bonding process is a solid liquid interdiffusion process (SLID) as described in previous chapters. The process itself comprises six stages: wetting, liquid diffusion and alloying, gradual solidification, solid-diffusion and equilibrium status. (Table 10)

Table 10. Sequence and steps of Au-Ga SLID bonding

Phase 1: Initial setup	**Phase 2: Wetting**	**Phase 3: Liquid diffusion and alloying**
Gold and gallium layers are prepared on substrate by deposition	Due to physical contact gallium wets surface of gold	Gold diffuses into liquid gallium until saturation
		
Phase 4: Gradual solidification	**Phase 5: Solid-Diffusion**	**Phase 6: Equilibrium**
The bond gradually solidifies by forming high melting point components	The bond is entirely solidified and all liquid disappeared	Equilibrium is reached according to the initial material volumes
		

To form the alloy with the chemical composition of $AuGa_2$ from formula 15 it can be calculated that the thickness relation between the gold and gallium film need to be 0.43; the thickness of the gold film should be 43% of the gallium film.

Beside the basic ability to form an alloy at low temperature, the time it takes for this reaction at the reaction temperature is important. The speed of alloy forming is mainly determined by diffusion processes.

According to the Fick's 2nd law (18) the diffusion in solid state can be described by the diffusion coefficient D that depends on concentration difference (*dc*) and time (*t*) and is specific for each material and temperature. In case of intermetallic systems, the

interdiffusion coefficient gives the important characteristic of the system. It can be experimentally determined. Marinković et al. did an intensive experimental investigation of interdiffusion coefficients of gold-based alloys (Marinković, et al., 1988). According to their result, the interdiffusion coefficient of gallium and gold to form $AuGa_2$ at 25°C is 1.6 x 10^{-12} cm²/s. From Figure 21 it can be clearly seen that D at 25°C for the formation of $AuGa_2$ is several orders of magnitude higher (10^{-12}cm²/s rather than 10^{-14}…10^{-20}cm²/s) than for other material combinations.

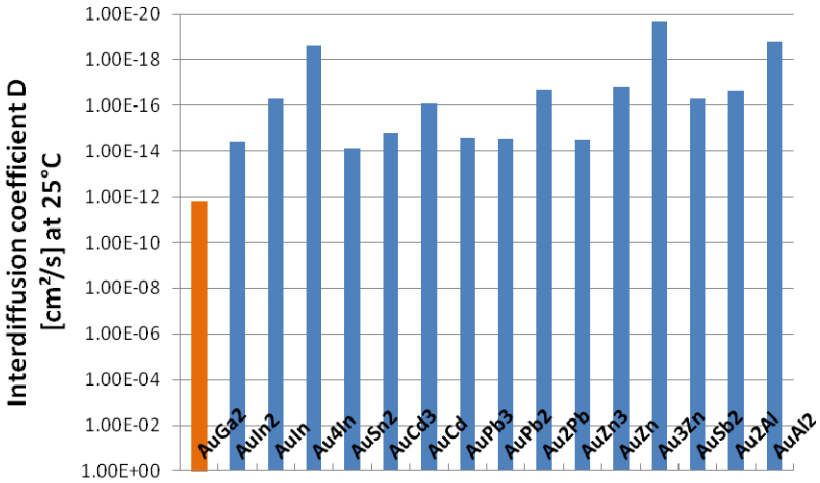


Figure 21. Interdiffusion coefficient D of different gold-based alloy formation (Marinković, et al., 1988)

$$\left\langle x^2 \right\rangle = \frac{A}{N}\int_{-\infty}^{+\infty} x^2 c(x,t)dx = 2Dt \qquad 21$$

With the 1D solution of Fick's law (Equation 21), the time *t* for formation of an alloy can be calculated. With x = diffusion length, D = diffusion coefficient, c = concentration, A = cross section area of diffusion and N is the number of source atoms per unit area initially placed at x = 0.
In the case of formation of $AuGa_2$ by 215nm gold and 500nm gallium, it can be formed in only about 5min at room temperature according to equation 21.

4.3.2 Experimental conditions and parameters

As can be seen in the binary phase diagram the first intermetallic phase from the gallium rich side is $AuGa_2$. This phase equals an alloy of gallium and gold with 66.6at.% of Gallium

(this is equivalent to 41.45mass%). For the thin film, it has been calculated from specific density of the materials that the film thickness of gold should be 43% of the film thickness of gallium. For practical purposes, it is important that the gold film thickness is no less than required to be sure that all gallium is used up during the bonding process, given that liquid gallium (melting point 30°C) in the interface would result in very low bonding strength. For the following bonding experiments, samples with a thickness of 1500nm and 500nm for gold and gallium respectively have been used. (Figure 22) Due to the excess of gold, it is expected that other phases with higher gold content than $AuGa_2$ will also be formed. Underneath the seed layer (gold) and the gold that is used for bonding chromium with 20nm thickness has been applied as an adhesion layer.

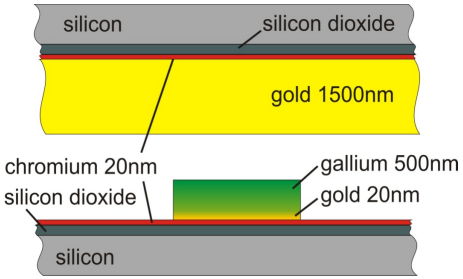


Figure 22. Setup and layer thicknesses for Au-Ga bonding experiment

4.3.3 Interface structure

As experimental conditions for first trial a temperature of 30°C, the melting point of gallium, and pressure of 15kPa for 20min has been chosen. Because the temperature is only slightly above room temperature and the pressure requirements are moderate no specialised equipment is necessary. The bonding experiment was done with a commercial wafer bonder from EV Group (EVG). With the described conditions, it was possible to successfully bond samples. After bonding, the bonding strength was found to be sufficient for further processing and handling. It was even possible to break the samples for cross sections without delaminating the bonding interface. The bond interface has been investigated by SEM to evaluate the success of the bonding and receive information on the mechanism of bonding, especially what intermetallic phases have been formed. In Figure 23 / Figure 24, a cross section of the resulting bond interface, achieved by mechanical breaking of the sample, is shown. What can be seen is that the gallium has been entirely consumed to form an alloy, whereas some part of the gold layer remains. The layer that has been formed from gallium and gold has interesting micro-structures that clearly shows crystallites and comprise several visible sections (Froemel, et al., 2012). By cutting the cross section of the bond interface with focused ion beam (FIB) 4 different sections (A, B, C

and D) can be identified from the optical impression. Section A is the remaining gold layer that was deposited on one side of the sample before bonding. The others (B, C and D) have different compositions of Au and Ga. The cross section was prepared by a gallium ion source; standard for FIB. In such a case, EDX measurement does not yield reliable result, because deposition from the ion source influences the composition.

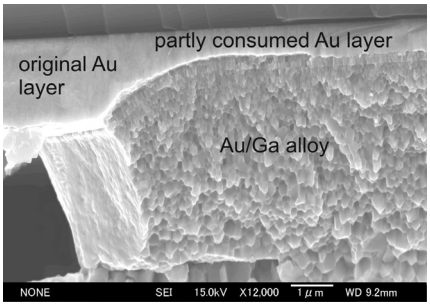


Figure 23. Cross section of gallium-gold bond interface achieved by breaking with visible alloy and partly remaining gold layer

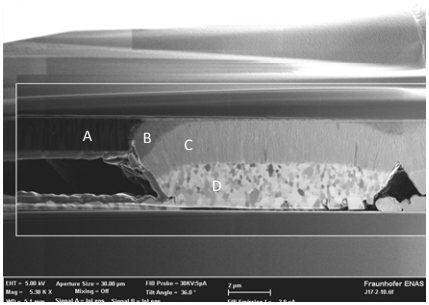


Figure 24. Cross section of gallium-gold bond interface achieved by focused ion beam (FIB) cutting to make several distinct different (A, B, C and D) sections visible

When separating the bond interfaces by shear or pull force, in case of cohesive failure, it is possible to obtain optical impression of the top view of one of the interface layers. Such a separated interface can be seen in Figure 25 and Figure 26. The interface failed in section D. The visible polygonal crystal structure is the same as reported for the $AuGa_2$ alloy in literature (Živković, et al., 2012).

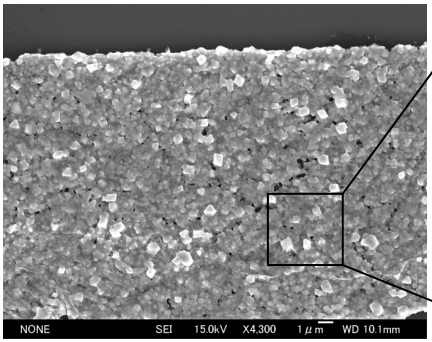


Figure 25. Top view of gallium-gold interface after separation by shear force (section D)

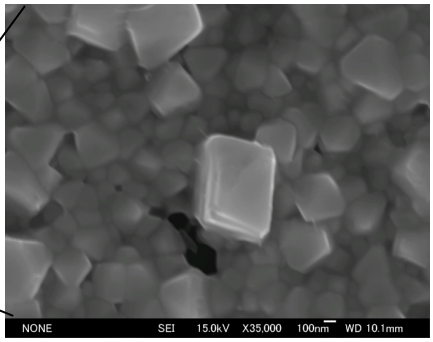


Figure 26. Clearly visible grain structure of cross section of gallium-gold interface (section D)

To fully characterise the material by EDX analytic measurements, cross sections by mechanical grinding and polishing have been done. In all the observations, the existence of

small and large voids became apparent. The measurement results showed contamination by silicon and carbon in the interface from the polishing process and carbon hydroxides in the air respectively. The results of the EDX measurements can be seen in Figure 27 - Figure 30.

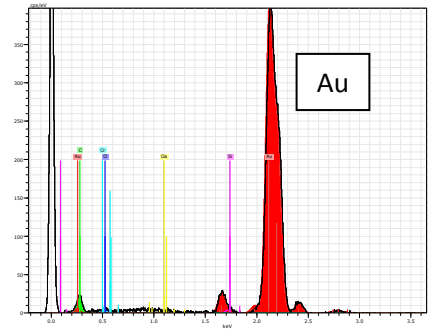


Figure 27. EDX spectrum at section A: 100wt.% Au

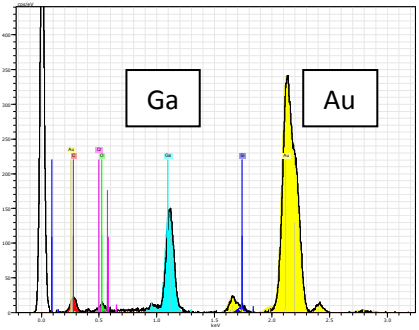


Figure 28. EDX spectrum at section B: 14wt.% Ga

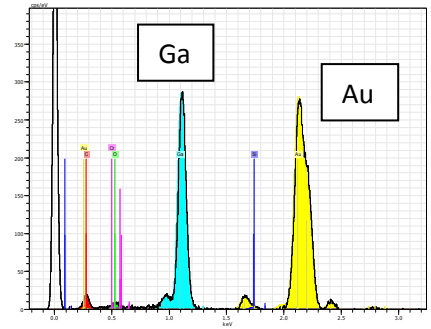


Figure 29. EDX spectrum at section C: 25.2wt.% Ga

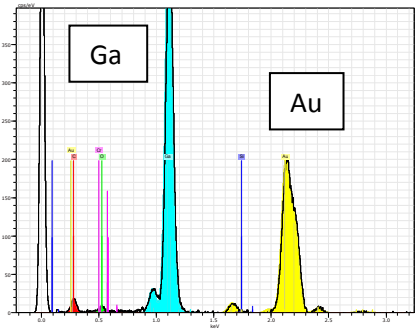


Figure 30. EDX spectrum at section D: 40wt.% Ga

Table 11. Calculation of atomic ratios of different section with EDX measurement results of Figure 27 - Figure 30 and densities of gold and gallium in Table 9.

section	wt.% / density Au	wt.% / density Ga	atomic ratio Au : Ga	attributed phase
A	100/19.32	-	1 : 0	Au
B	86/19.32	14/5.9	4.45 : 2.37	Au2Ga
C	74.8/19.32	25.2/5.9	3.87 : 4.27	AuGa
D	60/19.32	40/5.9	3.11 : 6.78	AuGa2

As can be seen in Table 11 all observed sections can be attributed to a certain intermetallic phase.

After the possibility of gallium-gold bonding has been essentially demonstrated, further experiments have been undertaken to investigate the interface stability dependence on temperature, fracture strengths and electric conductivity. For these experiments, samples with layer thickness according to Figure 31 have been used.
According to experiments at the temperatures used, Cr, Ti and Ta do not seem to take part in the alloying. All three can be used as adhesion layer for the gold. In the following cases, the adhesion layer for the gold is titanium.

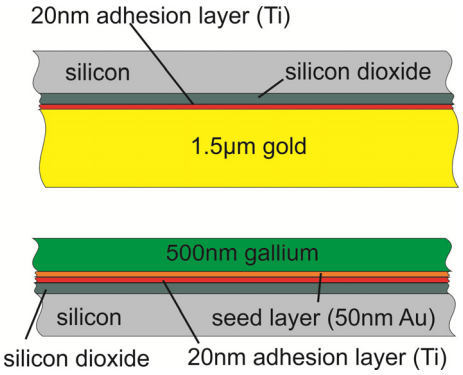


Figure 31. Layer setup for Au-Ga bonding experiment to investigate interface composition and stability

At first cross section was prepared from substrates bonded at room temperature. The bonding was done with commercial equipment EVG 520. Inside the bonding chamber <0.1Pa N_2 pressure was used, temperature 50°C and mechanical pressure was 3.5Mpa, applied for 10min.

4.3.3.1 Bonding at 50°C, no annealing

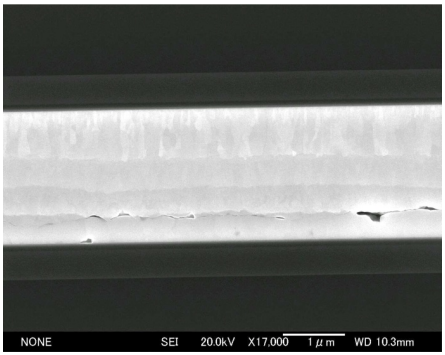


Figure 32. SEM picture of cross section of Au/Ga bond at 50°C without annealing

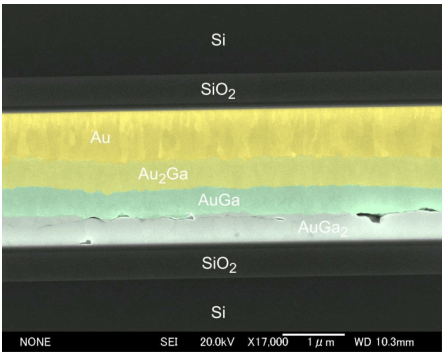


Figure 33. SEM picture of cross section of Au/Ga bond at 50°C without annealing, alloy composition highlighted by different colour

After bonding a cross section was done by ion cutting and the interface was observed by SEM and characterised by EDX. (Figure 32 and Figure 33) The result clearly shows the metal alloys in between silicon dioxide layers. The metal interface shows essentially the same characteristic as the result in Figure 24. It comprises four layers: a remaining gold layer as well as three intermetallic phases with composition of $AuGa_2$, AuGa and Au_2Ga respectively. Several sub-micrometre large voids can be observed in the $AuGa_2$ layer, especially near or at the interface to AuGa. These voids have small vertical dimensions (max. ~100nm), but have large horizontal dimensions (up to several µm).

4.3.3.2 Bonding at 50°C and annealing at 90°C for 80h

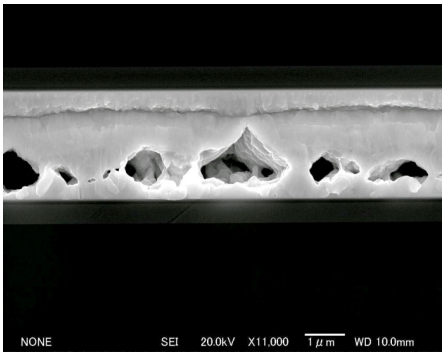


Figure 34. SEM picture of cross section of Au/Ga bond at 50°C and annealing at 90°C for 80h

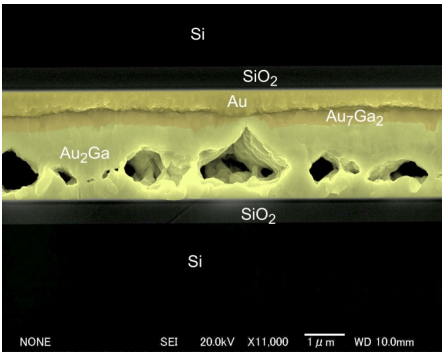


Figure 35. SEM picture of cross section of Au/Ga bond at 50°C and annealing at 90°C for 80h, alloy composition highlighted by different colour

With samples that have been annealed at 90°C for 80h after bonding that result changes. (Figure 34 and Figure 35) The composition of the interface has changed. $AuGa_2$ and AuGa phase are no longer present; instead, the Au_2Ga phase is now dominant. The remaining gold has decreased in volume and a new phase Au_7Ga_2 appeared in between Au and Au_2Ga. The volume of the voids has dramatically increased. The position essentially remains the same (at the previous AuGa/$AuGa_2$ interface, although they significantly extend in the direction of the gold layer. In some parts of the interface, the voids are almost entirely filling the gap in between the semiconductor substrates.

4.3.3.3 Bonding at 50°C and annealing at 145°C for 80h

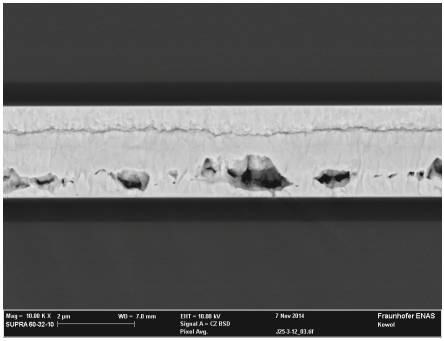


Figure 36. SEM picture of cross section of Au/Ga bond at 50°C and annealing at 145°C for 80h

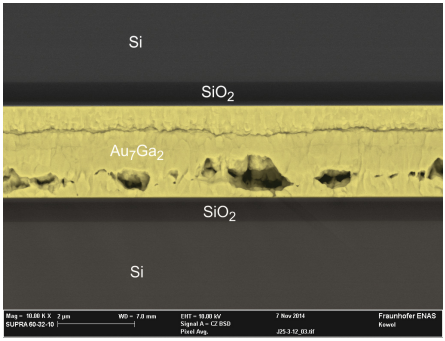


Figure 37. SEM picture of cross section of Au/Ga bond at 50°C and annealing at 1450°C for 80h, alloy composition

When the annealing temperature is increased to 145°C the interface entirely homogenises. (Figure 36 and Figure 37) Although the physical border to the previous gold layer remains visible, gold and gallium are now equally distributed, forming the intermetallic phase with the composition of Au_7Ga_2. (Figure 38) The previously observed voids did not significantly change in size or position. The void formation mechanism will be discussed in chapter 4.5. By further annealing at 200°C the result recorded after 145°C does not change, because the system is already in equilibrium.

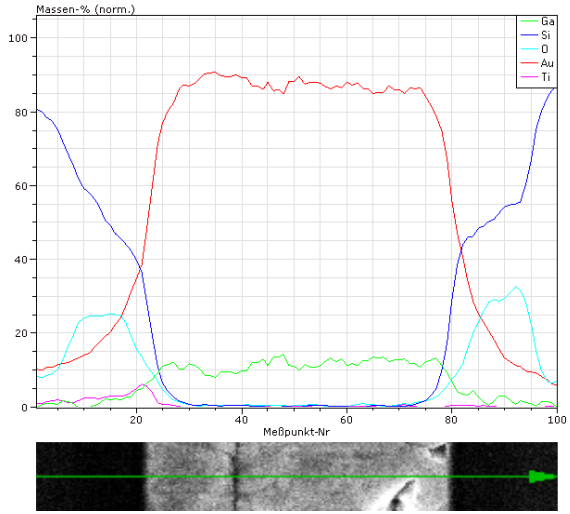


Figure 38. EDX line scan of the interface of Au/Ga bonded sample after 145°C annealing showing the complete homogenisation of the interface composition.

From the observation, it can be concluded that the alloying between gold and gallium starts at low temperature as expected. Immediately the intermetallic phase $AuGa_2$ is formed until all gallium has been used up. Additionally, AuGa and Au_2Ga phases come into existence in direction of the gold layer. Unused gold remains visible. With increasing temperature, Au_7Ga_2 forms and phases with higher gallium content, $AuGa_2$ and AuGa, dissolve. Ultimately, the entire interface has the single, homogeneous composition of Au_7Ga_2. Void formation starts at the interface between $AuGa_2$ and $AuGa_2$ phase (partly inside $AuGa_2$), already at a low temperature. During the transformation of these two phases to Au_2Ga, the voids significantly grow in the direction of higher Au concentration. The transformation of Au_2Ga to Au_7Ga_2 does not seem to have a significant impact on the voids.

4.3.4 Mechanical properties

To test the mechanical strength of Au/Ga bonds, oxidised (500nm SiO_2) silicon chips (2cm x 2cm) have been coated with gold respective gallium. Gold was sputtered with an adhesion layer of titanium by magnetron sputtering in situ with 300W power at 0.5Pa argon pressure. Gold thickness was 1.5µm with 20nm titanium. 0.5µm Gallium was deposited by electroplating (see chapter 2.1.3 for parameters and conditions) on a 50nm gold seed layer with 20nm titanium adhesion layer. As bonding parameters for all samples, the following conditions have been used: 2000N, 50°C, 20min at <1Pa N_2 pressure. The bonding equipment was an EVG 520 commercial wafer bonder. The chips were diced after bonding

into 5mm x 2.5mm dies. To obtain information on the temperature stability and morphologic changes in the bond interface depended on temperature samples have been annealed at different temperatures (50°C, 90°C, 145° and 200°C) for 80h. After that shear test took place. For details on the test equipment and test parameters please refer to chapter 3.1.

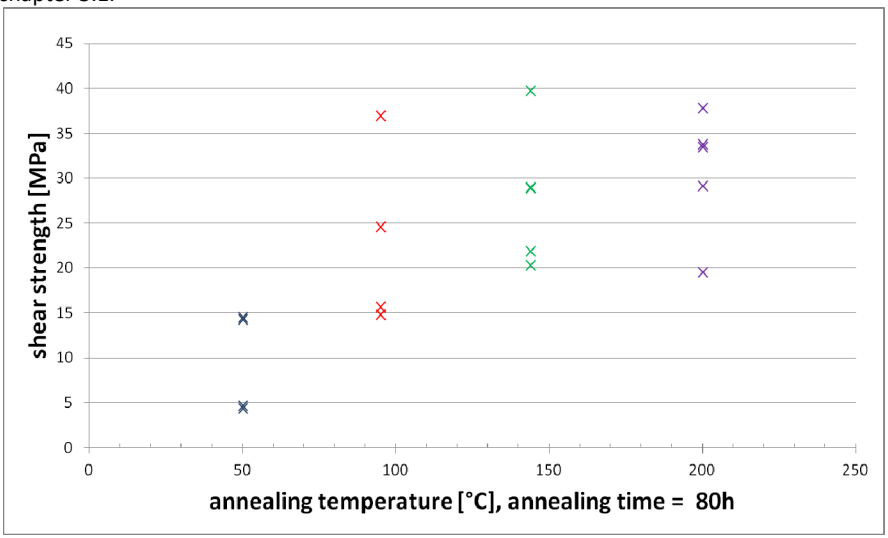


Figure 39. Results of shear strength measurement of bonded Au/Ga samples in dependence of annealing temperature

The shear test result shows very weak shear strength after 50°C temperature that is essentially also the bonding temperature. Shear strength is increasing strongly at 90°C and them slightly at 145°C. (Figure 39)

Table 12 . Average shear strength of samples bonded Au/Ga at 50°C annealed at different temperatures

annealing temperature	average shear strength
50°C	9.4MPa
90°C	18.4MPa
145°	27.9MPa
200°	30.6MPa

Overall, the strength remains weak (Table 12). For comparison, glass frit bonded samples can achieve up to 50MPa (Vogel, et al., 2012). The increase from between 50°C and 90°C is attributed to the elimination of $AuGa_2$. From existing literature, it is known that this phase is brittle. (Fischer-Buehner, et al., 2010) Additionally the spread of values is quite high, which is related to the voids. The void concentration is very different at some parts of the

interface it is with some (large) voids, other parts essentially comprises voids. Between 145°C and 200°C there is almost no change, that is conform to the interface composition data, because the interface is already homogenised at 145°C.

4.3.5 Electrical properties

Electric conductivity/resistivity of a bonded contact is, beside the shear strength, of high interest. In case of application in the field of 3D integration and stacking of devices, vertical electrical contacts are necessary.
For the measurements sample structures according to chapter 3.2 have been prepared. These samples have been bonded with a commercial wafer bonder EVG 520, all of them with the same parameter: 50°C, 2000N mechanical force, 20min, and <1Pa N_2. After measuring the initial resistance, the samples have been annealed at different temperatures. During the annealing process, electrical resistance of the samples was measured periodically. The resistivity was calculated based upon the result. (Figure 40)

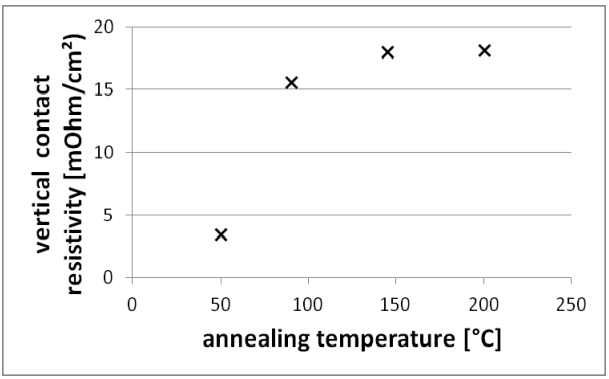


Figure 40. Contact resistivity of vertical bonded contacts between two wafers with gold and gallium after annealing at different temperatures

The vertical resistivity of the contacts starts after bonding at $3.5 \times 10^{-4} \Omega/cm^2$. After annealing at 90°C, it increases about 5-times to $15.5 \times 10^{-4} \Omega/cm^2$. Further temperature increase yields only slight changes of resistivity that seems to level off. Overall, the conductivities are rather poor; for comparison, bulk gold has a resistivity at room temperature of $2 \times 10^{-8} \Omega/cm^2$ (Matula, 1979).

4.3.6 Hermeticity

It has been decided to use the optical leak rate measurement technique described in chapter 3.3.5. This technique has the advantage of easy test structure fabrication and simple measurement. To investigate the hermeticity properties of gallium-gold bonds special test structures have been prepared. These test structures essentially comprises enclosed cavities with a membrane. (Figure 41 and Figure 42)

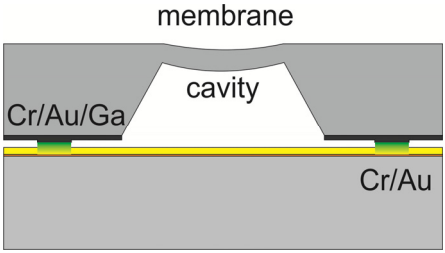


Figure 41. Schematic cross section of test structure for hermeticity testing; cavity wafer with structured gallium on gold/titanium seed layer, and wafer with unstructured gold and adhesion layer chromium.

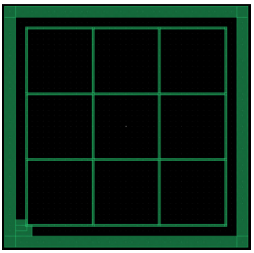


Figure 42. Mask design for the hermeticity bond test, bond frame layer. The outer large frame is only for rough mask alignment. The lower left corner structure is for electrical contact during electroplating. Bond frame with is 200µm.

Fabrication of these test structures includes two wafers, one with cavities and one to enclose the cavity by bonding.

a)  	The cavity wafer is made of a double side polished silicon wafer with 50µm thickness, prepared by wet thermal oxidation, resulting in 1µm thick silicon dioxide that will later be used as etch mask for the cavity fabrication.
b)  	On one side of the future cavity wafer gold layer is sputtered with chromium adhesion layer. Parameters for magnetron sputtering are: 5Pa chamber pressure (argon flow), not heated sample holder and 300W RF power. The chromium layer is sputtered with 20nm thickness; the gold layer has 50nm thickness. The purpose of this layer is to work as a seed layer for the gallium electroplating.

c)  	The previously deposited Au/Cr seed layer is structured by lithography. This parameters have been used: HMDS spin on, 20s at 3000rpm bake at 90°C, 1min spin on OFPR800 15cp, 20s at 3000rpm bake at 110°C, 90s hotplate exposure with 44mJ/cm² development by NMD-3, 80s Au etching by Aurum 302, 3.5 min Cr etching by KMnO4 : NaOH : H2O, 2 : 3 : 12 , 10 s
d) 	The next step is etching of the silicon dioxide on one side of the wafer to finish the mask for the next silicon etching. The photo lithography used the same parameter like in step c). SiO2 etching was done by HF:NH4F = 9:100 solution, 10 min. The resist has been removed by MS2001, 60°C, 5 min. The opening in the mask layer is 3mm x 3mm, square size.
e) 	To form the membrane that is necessary for the measurement silicon is etched by wet etching. It was chosen to use 25% tetramethylammoniumhydroxide (TMAH) solution. It has the advantage of high selectivity to silicon dioxide so that Si3N4 has not necessarily to be used as etch mask. Etching was done at 80°C for 110min, resulting in 335µm depth. It should be noted that although TMAH etches anisotropic, but the angle is not the same as in case of KOH, because the selectivity between (100) and (111) is not as high.

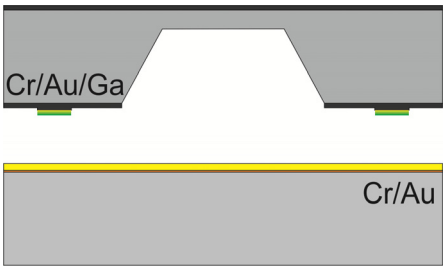
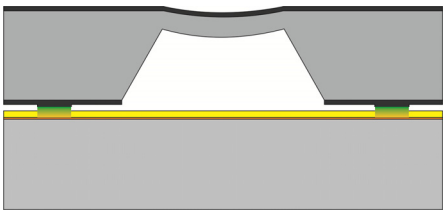
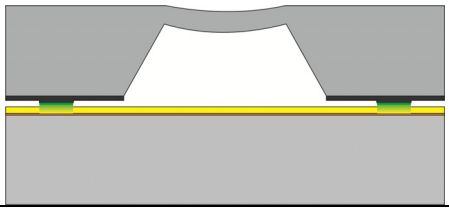
f)  	After forming the membrane by wet etching, gallium has been deposited on the gold seed layer. This has been done with the electroplating setup described in chapter 2.1.3., resulting in a layer thickness of 0.5µm. Seed layer etching or lithography was not needed, because the seed layer is already structured.
g)  	A second wafer has been prepared to close the cavity by bonding between gallium and gold. A thicker layer of gold including a chromium adhesion layer has been deposited on this wafter by magnetron sputtering. As in step b) 300W RF power, as well as 5Pa chamber pressure under argon flow was used. The layer thickness of chromium is 20nm and gold is 1.5µm thick. One side of the wafer is entirely covered with gold.
h) 	The next step is the bonding of the cavity wafer with the cover wafer. No preparation is necessary; the gold surface as well as the gallium surface is ready for bonding without pre-treatment. Since the gold layer is not structured, no alignment is necessary to bond. The bonding was done with commercial equipment EVG 520. Inside the bonding chamber 0.1Pa N2 pressure was used, temperature 25°C and mechanical pressure was 3.5Mpa, applied for 10min.
i) 	The last step was the removal of the remaining SiO2 on top of the cavity wafer. This has been done by ICP dry etching using CHF3 as etch gas under 5Pa pressure with 60W RF power for 10 min. This has been done to prevent influence on the membrane deflection by the silicon dioxide.

Figure 43a-i. Schematic process sequence for fabrication of test structure for hermetic testing of bonds

According to the sequence described in Figure 43, six test wafer pairs have been made, with each containing nine test structures. Bonding was originally done at a temperature of 25°C and the mechanical pressure was 3.5Mpa. No annealing after bonding took place. No visible membrane deflection could be observed.

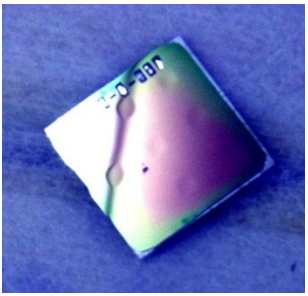


Figure 44. Cavity test structure directly after Ga/Au bonding (7MPa mechanical pressure and 2mm bond frame)

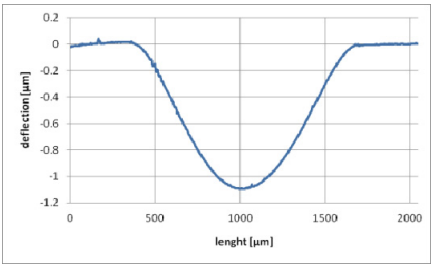


Figure 45. Membrane bending directly after bonding for test structure depicted in Figure 44

Furthermore, it was tried to improve the conditions by doubling the mechanical pressure up to 7MPa as well as to anneal the samples after bonding at 200°C for 20h. However, even after that treatment the hermeticity properties did not improve. In addition, it was tried to increase the bonding area up to 2mm wide bond frame. This finally resulted in visible membrane deflection. (Figure 44 and Figure 45) However, after a maximum one-week storage time, all such samples no longer showed any deflection. Even that very wide bond frame did not result in satisfactory gas permeability properties.
It can be concluded that for Ga/Au bonding it is very difficult to achieve hermetic conditions. Explanation can be found in the formation of extremely large void that could be observed in the interface cross sections. These voids do not prevent mechanical bonding but open up easy ways for gas to move through the bonding frame.

4.3.7 Summary and discussion Au/Ga bonding

The experiments revealed one major property of Au/Ga bonding: the massive formation of small and large voids. Since this void will reduce the effective bonding area, their existence has the effect of lower overall bonding strength. Furthermore, they prevent hermetic bonding. The explanation for these voids could be a difference in density between gold, gallium and its solid intermetallic phases.

Table 13: density of selected phases Au/Ga binary system

material	density
Au	19.29g/cm³
Au7Ga2	16.73 g/cm³
Au2Ga	15.26g/cm³
AuGa	12.77g/cm³
AuGa2	9.96g/cm³
Ga	5.904g/cm³

During the alloying the density (Table 13) of the gallium containing alloys becomes higher and the volume subsequently smaller. With the following calculation, the effect shall be quantified and rated. The volume V with mass m and density ρ can be calculated by:

$$V = \frac{m}{\rho} \qquad 22$$

By using a one-dimensional system, it can be changed to:

$$h = \frac{m_A}{\rho} \qquad 23$$

h is the height of the interface layer, and m_A is specific area mass [g/cm²]. Under the assumption of Au_7Ga_2 as the target for equilibrium composition after bonding, according to Formula 15 the thickness ratio between gold and gallium shall be 3; therefore, e.g. 1.5µm gold and 500nm gallium is necessary.
In that case by using Formula 23 m_{AAu} = 2.8935e10-3g/cm² and m_{AGa} = 0.2952e10-3g/cm². The mass of the final Au_7Ga_2 alloy is the sum of the terminal phases $m_{AAu2Ga} = m_{AAu} + m_{AGa}$ = 3.18e10-3g/cm². By applying this area-specific mass and the density of Au_7Ga_2 to Formula 23 the resulting height of the Au_7Ga_2 layer h_{Au7Ga2} = 1.9µm. This is 90% of the original height of gold and gallium. A volume change of 10% is relatively high, for example Cu/Sn (Cu_6Sn_5) has 6.83% shrinkage. For such bonding technologies, very large voids like in the case of Au/Ga are not reported. As an additional reason for the void formation, the Kirkendall Effect is considered; that will be discussed in chapter 4.5.

In the following, all test results (electric, mechanic and structural) of Au/Ga will be compared, checked for validity and interpreted. In Figure 46 electric and mechanic properties are shown in one diagram.
From the structural interface data, the most important change from 50°C annealing temperature to 90°C annealing temperature is the extensive formation of voids. Consequently the conductivity significantly dropped, which is related to the fact that the electric active vertical cross section decreases due to the large voids. The shear strength

increases at the same time although the large voids are formed. This is attributed to the elimination of the $AuGa_2$ phase. $AuGa_2$ is known as brittle with low mechanical strength. (Fischer-Buehner, et al., 2010). Between 90°C and 145°C, the shear strength significantly increases, although resistivity only shows a small change. At the same time, the interface structure (voids) does not change, but the composition becomes different. Au_2Ga is transformed to Au_7Ga_2. The higher gold content leads to better conductivity and mechanical strength of Au_7Ga_2 seems much higher than Au_2Ga. (Froemel, et al., 2013)

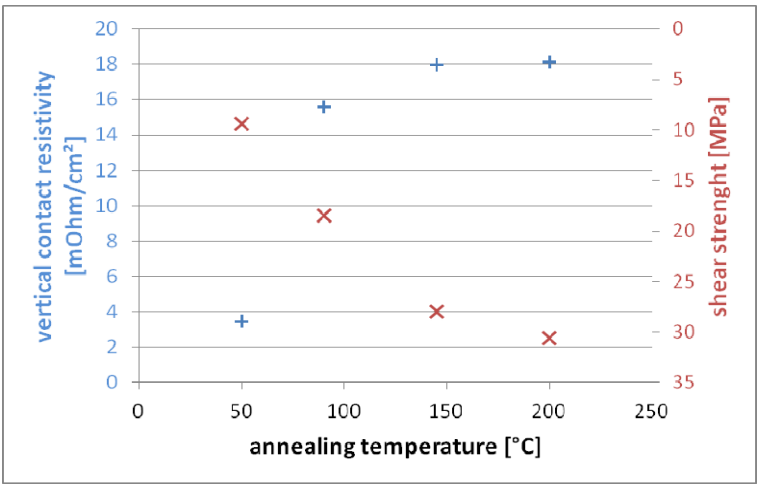


Figure 46. Display of electric and mechanic parameters of Au/Ga bonds in relation to annealing temperature.

4.4 Gallium – copper SLID bond process

As described in 5.1, the alloying of gallium and copper in the form of amalgams for dentistry as well as solder for mechanical engineering are known since considerable time. It is only logical to investigate the application of such material combination for wafer bonding with electroplated thin films.

4.4.1 Theory

Gallium and copper exhibit a rather complex phase diagram with nine solid intermetallic phases (Figure 47).

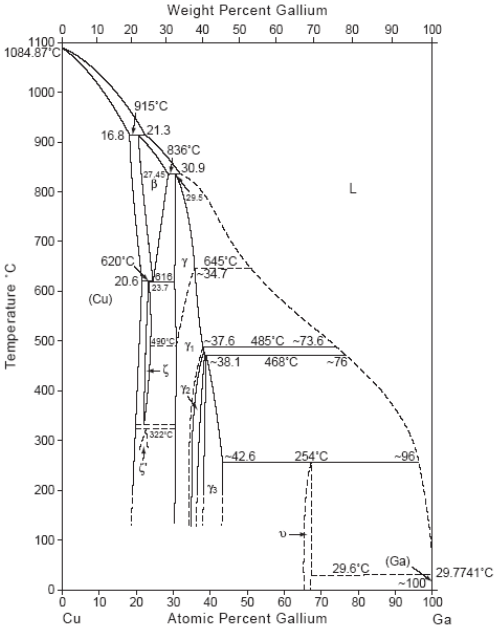


Figure 47. Cu/Ga binary phase diagram (Massalski, 1986)

The intermetallic phase with the most low transformation point is $CuGa_2$ with 254°C. It is the phase with the lowest copper content. Phases with higher copper content have more high transformation points. According to Ancharov et al. when alloying gallium and copper at 25°C always $CuGa_2$ intermetallic phase is formed first, independent from initial composition. (Ancharov, et al., 2008) Subsequently, other phases can be formed to reach equilibrium. To form the alloy with the chemical composition of $CuGa_2$ from formula 15, it can be calculated that the thickness relation between the copper and gallium film need to be 0.3, whereby the thickness of the copper film should be 30% of the gallium film.

Table 14: Overview interdiffusion coefficients of different gallium alloys (Marinković, et al., 1992)

material system	compound formed	melting/transformation temperature of compound	interdiffusion coefficient
Ag-Ga	Ag3Ga	425°C	4.4 x 10-13cm²/s
Au-Ga	AuGa2	491°C	1.6 x 10-12cm²/s
Cu-Ga	CuGa2	254°C	3.1 x 10-15cm²/s
Pd-Ga	PdGa5	200°C	1.6 x 10-16cm²/s

By using the 1D solution of Fick's law (equation 21), the time for formation of an alloy can be calculated. In the case of formation of $CuGa_2$ by 150nm copper and 500nm gallium, it can be formed in about 20h at room temperature. Table 14 shows a comparison of interdiffusion coefficients of different gallium alloys.

4.4.2 Experimental conditions and parameters

Cu_9Ga_4 intermetallic phase has a transformation temperature of at least 468°C, which is more than sufficient for most applications in semiconductor wafer bonding. This phase is preferred compared to $CuGa_2$ with a transformation point of 254°C. To achieve Cu_9Ga_4 a ratio of 1.35 copper thickness vs. gallium thickness needs to be set up according to formula 15. This equals a composition of 32.9wt.% gallium. Bykow et al. experimented with different compositions of gallium and copper. They annealed their bulk samples up to 1300K and subsequently checked the phase composition. Between 32wt.% and 38wt.% gallium, the result was always Cu_9Ga_4. (Phase Equilibrium in Binary System Cu-Ga, 2012) It can be assumed this phase composition is even stable at a high temperature. To achieve this phase for the bonding experiment between copper and gallium, a setup with 1.35 µm thick copper and 1µm gallium has been chosen. (Figure 48)

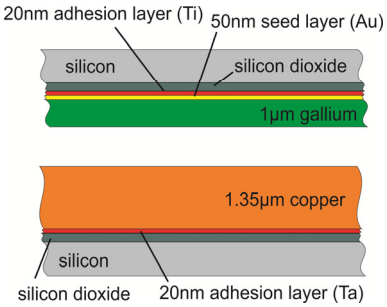


Figure 48. Layer setup for bonding experiments with copper-gallium

4.4.3 Interface structure

To investigate the bond interface composition and its behaviour over temperature samples with the layer composition described in the previous section have been fabricated. The samples have been bonded in a commercial wafer bond system EVG 520 with these parameters: 25°C, 20min, 2000N, and <1Pa N_2 pressure. After the bonding, annealing was done with different samples at different temperatures: 50°C, 90°C, 145°C and 200°C. Annealing time was always 80h. To remove the copper oxide before bonding a dip was

done in citric acid ($C_6H_8O_7$) for 1min and subsequent DI-water rinse. More information about copper pre-treatment can be found in chapter 4.4.4.
The bonded samples have been cut by ion cutting to make a cross section of the interface. By SEM observation and EXD measurement the interface could be observed and characterised.

4.4.3.1 Bonding at 25°C without further annealing

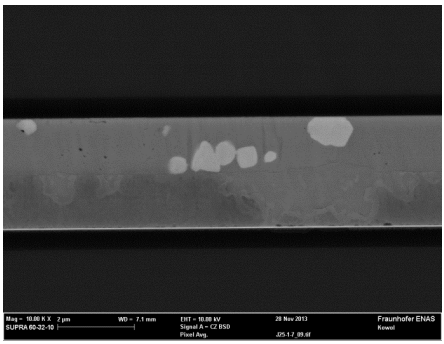


Figure 49. SEM picture of cross section of Cu/Ga bond at 25°C without annealing

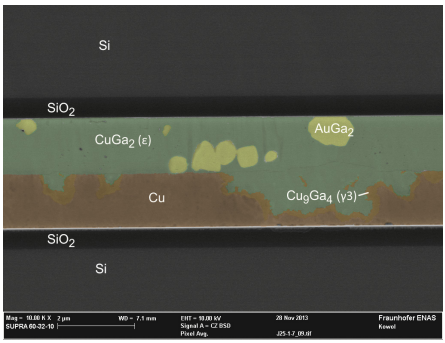


Figure 50. SEM picture of cross section of Cu/Ga bond at 25°C without annealing, alloy composition highlighted by different colour

The cross sections of samples that have been brought into contact at room temperature show the existence of four different solid intermetallic phases. (Figure 49 and Figure 50) No pure gallium could be observed, the gallium seems entirely used up or in solution. Most part of it has formed together with copper the ε-phase of the Cu-Ga system. The ε-phase is an intermediate solid solution that has an approximate composition of $CuGa_2$. Furthermore, clusters of $AuGa_2$ intermetallic compound can be observed embedded into the ε-phase. Some of the $AuGa_2$ clusters are located at the interface between the ε-phase and silicon dioxide; however, some of them can also be found at other locations inside the $CuGa_2$ phase. The $AuGa_2$ phase clusters are believed to have formed from the seed layer of 50nm gold.
Copper is present in large quantities, at some points the original surface still exists, at other points phase transformation occurred. At most areas at the interface between copper and the ε-phase, another phase can be seen. It is believed that this is an intermediate solid solution with the approximate composition of Cu_9Ga_4, and specifically the γ_3-phase. Moreover, small and large voids can occasionally be found in the ε-phase.

4.4.3.2 Bonding at 25°C and annealing at 50°C for 80h

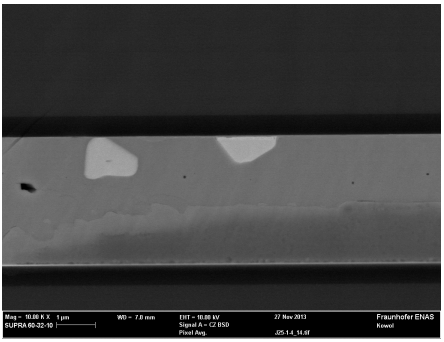


Figure 51. SEM picture of cross section of Cu/Ga bond at 25°C and annealing at 50°C for 80h

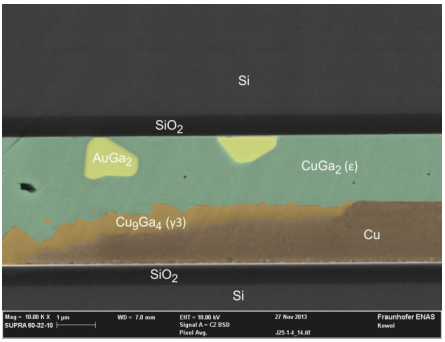


Figure 52. SEM picture of cross section of Cu/Ga bond at 25°C and annealing at 50°C for 80h, alloy composition highlighted by different colour

In case annealing is being done at 50°C for 80h the interface does not significantly change. (Figure 51 and Figure 52) Still there is a large amount of $CuGa_2$. EXD measurements suggest that there is no longer gallium in solution. Similar to the non-annealed samples, at some points there is no Cu_9Ga_4 phase in between Cu and $CuGa_2$. Nonetheless, usually no void can be observed at such location. The copper layer is largely intact, with some of it used up for alloying with gallium.

4.4.3.3 Bonding at 25°C and annealing at 90°C for 80h

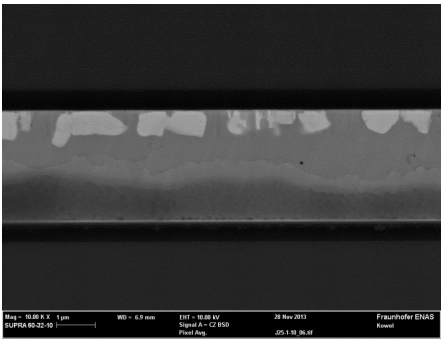


Figure 53. SEM picture of cross section of Cu/Ga bond at 25°C and annealing at 90°C for 80h

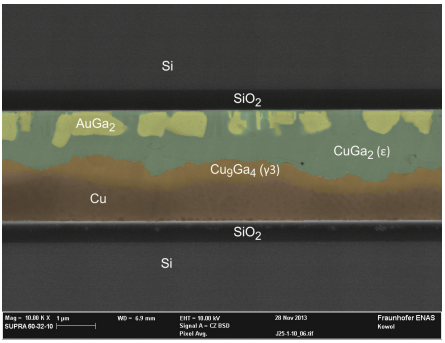


Figure 54. SEM picture of cross section of Cu/Ga bond at 25°C and annealing at 90°C for 80h, alloy composition highlighted by different colour

After annealing at 90°C for 80 hours, the SEM observation of bonded samples reveal the same basic composition as samples without annealing and annealing at 50°C for 80h. (Figure 53 and Figure 54) The $AuGa_2$ intermetallic compound clusters are still located inside the ε-phase. The original surface of the copper layer can no longer be recognised; instead, a layer that seems composed of the γ_3-phase can be seen everywhere. The occurrence of previously observed voids does not change in size or number.

4.4.3.4 Bonding at 25°C and annealing at 145°C for 80h

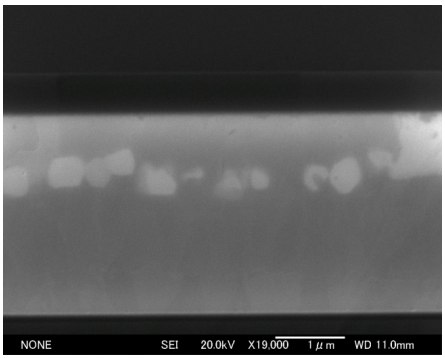


Figure 55. SEM picture of cross section of Cu/Ga bond at 25°C and annealing at 145°C for 80h composition highlighted by different colour

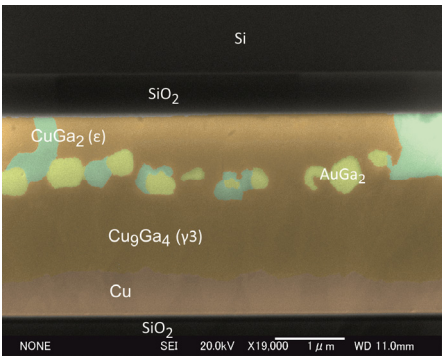


Figure 56. SEM picture of cross section of Cu/Ga bond at 25°C and annealing at 145°C for 80h, alloy composition highlighted by different colour

Cross sections taken from samples after annealing at 145°C for 80h show a large reduction of size of copper. (Figure 55 and Figure 56) Furthermore, there is almost no $CuGa_2$ phase left; instead, the area of the previous copper layer and $CuGa_2$ phase is now covered by an intermediate solid solution with approximate composition of Cu_9Ga_4. According to EDX measurements, it seems the γ_3-phase. Some of ε-phase remains present with $AuGa_2$ clusters in it. The $AuGa_2$ clusters are now partly incorporated into the Cu_9Ga_4 phase that replaced the ε-phase. The size and number of voids have slightly increased. This could be explained by a density difference between the ε-phase and γ-phase. Since both phases are solid, a higher bond pressure could not entirely prevent this void formation.

4.4.3.5 Bonding at 25°C and annealing at 200°C for 80h

Figure 57. SEM picture of cross section of Cu/Ga bond at 25°C and annealing at 200°C for 80h composition

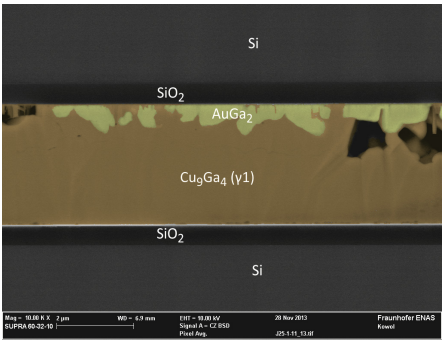
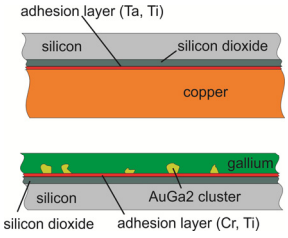
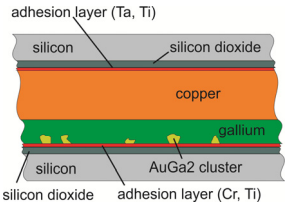
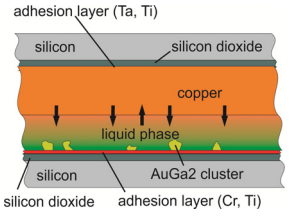
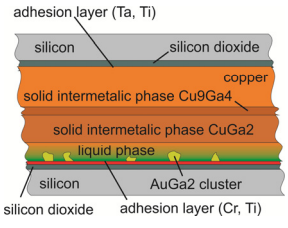
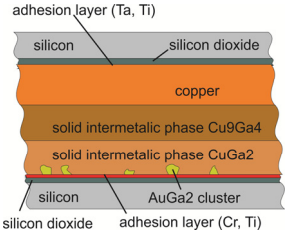
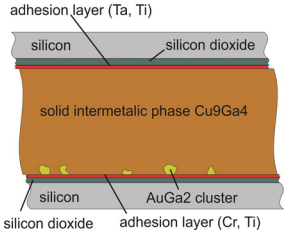


Figure 58. SEM picture of cross section of Cu/Ga bond at 25°C and annealing at 200°C for 80h, alloy composition highlighted by different colour

Further annealing at 200°C for 80h shows a very different picture compared to lower temperatures. The ε-phase can no longer be found; instead, the entire bond interface comprises a solid solution with about Cu_9Ga_4 composition. In addition to the γ3-phase, the γ1-phase also seems present in the majority. The $AuGa_2$ clusters still exist, albeit now entirely enclosed by the Cu_9Ga_4 phase. (Figure 57 and Figure 58) The size and number of voids have further slightly increased. The copper terminal phase is entirely used up now.

According to the findings by SEM, cross sections taken from samples annealed at different temperatures after bonding a model for what is going on will be presented in Table 15.

Table 15. Sequence and steps of Cu-Ga SLID bonding according to cross section analysis. In brackets are the corresponding temperatures.

Phase 1: Initial setup	**Phase 2: Wetting**	**Phase 3: Liquid diffusion and alloying (room temperature)**
copper and gallium layers are prepared on substrate by deposition	due to physical contact gallium wets surface of copper	copper diffuses into liquid gallium until saturation
		
Phase 4: Gradual solidification (room temperature)	**Phase 5: Solid-Diffusion (50°C – 145°C)**	**Phase 6: Equilibrium (200°C)**
at the interface between Cu and Ga Cu_9Ga_4 and $CuGa_2$ are solidifying	after all gallium has been used up Cu_9Cu_4 phase is expanding and consuming Cu and $CuGa_2$	Equilibrium is reached by complete formation of Cu_9Cu_4 phase
		

4.4.4 Surface pre-treatment

To obtain successful diffusion between different materials no diffusion hindering substances must be located in the interface. Oxides typically prevent such interdiffusion. Almost all metals do form spontaneously an oxide even at room temperature when subjected to oxygen, e.g. in air. (Mott, 1940) For copper, this has been extensively investigated also in relation to applications in form of thin films. It has been found that at temperatures below 200°C mainly Cu_2O is being formed that further oxidises to CuO. (Lawless, et al., 1956). When applications in the field of microelectronics became apparent, methods to control the oxidation of copper needed to be developed. Successful

approaches include alloying copper with Cr, Pd, Ti or Al and covering the copper with Si_3N4 or Cu_3N. (Li, et al., 1991)
Additionally to the need to protect the corrosion of copper by oxidation, during the development of SLID bonding between copper and tin, the need to remove existing copper oxide also arose, with several methods having been considered.

4.4.4.1 Surface treatment by liquid etchant

In this case, the surface of the copper is treated with a chemical in its liquid phase that etches the copper oxide just before the bonding. Such pre-treatment is quite commonly used nowadays and is applied with high yield and reliability in industrial production. Currently citric acid ($C_6H_8O_7$) and acetic acid (CH_3COOH) are the preferred etchants for most applications (Sood, et al., 2010), (Jang, et al., 2009). Such kind of treatment has been used for the experiments in chapter 4.4.3. As can be seen in this chapter it can be successfully applied. However, it has the significant disadvantage of all liquid treatments, whereby most micromechanical structures will be damaged either by the viscous flow during the treatment or the sticking effect that happens during drying after the treatment due to capillary forces. A way to avoid the sticking is the use of a super critical point dryer that uses the equality in density of liquid CO_2 and its gaseous phase at 304.25K and 7.39MPa to avoid the capillary effect.

4.4.4.2 Surface treatment by chemicals in their vapour phase

To entirely avoid the negative effects of liquid chemicals, it is also possible to use chemical agents that effective in their vapour phase. Much professional wafer bond equipment has recently been with formic acid (HCOOH) treatment units. These units generally bubble nitrogen through liquid formic acid and subsequently let it stream over the bonded wafers in the bonding chamber. Although it seems obvious that the copper oxide is not etched by the formic acid, the mechanism is very different. Formic acid is decomposing itself at higher temperatures into CO_2 and H_2, which is facilitated on metal surfaces by a catalytic effect. The released hydrogen subsequently reduces the copper oxide on the surface. Both the decomposition of formic acid and the reduction of copper oxide require temperatures higher than 200°C. Whereas this technology can be easily applied for wafer bond technologies that require high bonding temperatures like thermo-compression bonding, for bonding technologies near room temperature it will offset the low temperature budget advantage.

4.4.4.3 Annealing in hydrogen atmosphere

Like in the formic acid vapour phase, treatment the copper oxide is reduced by hydrogen directly inside the bonding equipment before bonding. To exclude the possibility of catastrophic explosion by reaction with oxygen of air rather than pure hydrogen gas, so-called forming gas is typically used. Forming gas usually comprises nitrogen with less than 10% hydrogen. In that case, the hydrogen concentration near the copper oxide surface is usually lower than by decomposition of formic acid. In addition, the reduction works only at higher temperatures and thus has the same disadvantage.

4.4.4.4 In situ treatment by plasma or ion beam

Of course, it is also possible to remove copper oxide by either plasma etching processes. These chemical etching processes are the same that are used for copper structuring and are based upon chlorine. To prevent the reoxidation of copper, such a process needs to be done in bonding equipment or a setup coupled to the bonding equipment by an uninterrupted vacuum track. At present, no such setup is commercially available. Besides the chemical etching, also physical etching by ion beam is possible. Because such ion etching effect for atomically cleaning a surface is used in surface activated bonding, bonding equipment including such pre-treatment is available. (Higurashi, et al., 2009)

4.4.4.5 Covering of copper surface with an oxygen impenetrable layer

For some applications, it might be difficult to use the previous described pre-treatment processes, especially in case they are involving liquids. To find an alternative the possibility to use a non-oxidising cover layer on top of the copper to prevent oxidising of the copper was investigated. This cover layer must not hinder the copper-gallium alloying process. It was decided to use gold as a cover layer. It easily alloys with gallium, is already used a seed layer for the gallium electroplating and does not form a stable oxide. The gold layer was sputtered in situ in the same sputter equipment directly after sputtering the copper layer without breaking the vacuum. Thickness was 60nm sputtered at 300W with 0.5Pa argon pressure. (Figure 59)

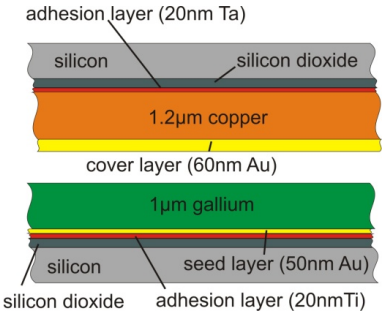


Figure 59. Experimental setup to test the application of a gold cover layer to prevent the oxidation of copper

Bonding was done with such a gold cover layer at 25°C, force: 1000N, atmosphere: N_2 1Pa, time 10min. This are the same bonding parameters like bonding with liquid pre-treatment that have been done previously. Dicing into 2mm x 2mm chips after bonding with a resulting yield of >90% showed the effectiveness of this method. To investigate the temperature behaviour the samples have been annealed up to 200°C for 80h and the cross section was observed by SEM and EDX. (Figure 60, Figure 61, Figure 62, and Figure 63)

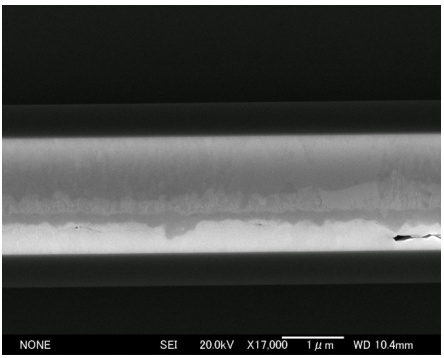


Figure 60. SEM picture of cross section of Cu/Ga bond at 25°C after annealing at 50°C with gold protective layer according to Figure 59

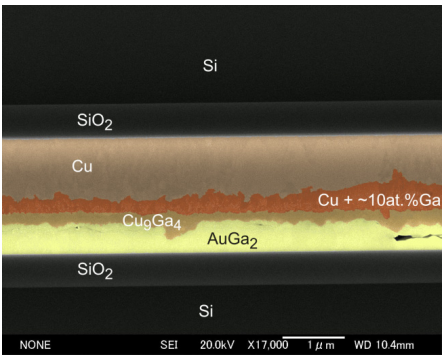


Figure 61. SEM picture of cross section of Cu/Ga bond at 25°C after annealing at 50°C with gold protective layer according to Figure 59 (composition highlighted with colour and named)

The composition analysis shows several differences compared to the experiments with just wet treatment of copper prior bonding. $AuGa_2$ phase apparently also exist, although rather than locally in Cu/Ga phases distributed $AuGa_2$ clusters it forms a full layer up to several 100nm and is located at the SiO_2 interface. This can be attributed to the fact that the amount of gold is much larger this time. In the previous experiment without the cover layer gold was only present in form of a 20nm thin seed layer. Whereas this time additionally 60nm on the copper was existent. Occasionally small voids (lengths up to 2µm,

height up to 100nm) could be observed in the $AuGa_2$ layer. They are similar in frequency compared to voids without gold layer, but significant smaller in size. Next to the $AuGa_2$, a layer of Cu_9Ga_4 similar in size to previous experiments exists. Remarkably, even at 50°C, the $CuGa_2$ phase does not exist. Moreover, a thin layer mainly comprising copper with a gallium content of up to 10at.% is visible in between the Cu_9Ga_4 layer and copper.

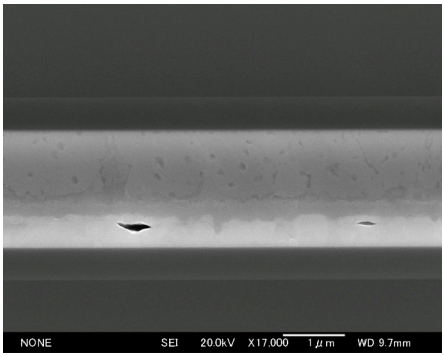


Figure 62. SEM picture of cross section of Cu/Ga bond at 25°C after annealing at 200°C with gold protective layer according to Figure 59

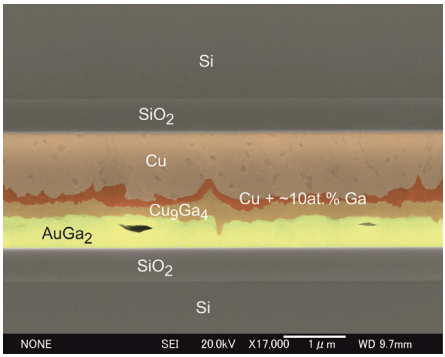


Figure 63. SEM picture of cross section of Cu/Ga bond at 25°C after annealing at 200°C with gold protective layer according to Figure 59 (composition highlighted with colour and named)

The different composition of the interface is a clear indication that the existence of the gold layer in between copper and gallium changes the diffusion and solidification behaviour during bonding. After annealing at 200°C for 80h the interface does essentially not change. It shows the same composition. That seems logical considering the fact that the main change during annealing at different temperatures in case of wet chemical pre-treatment of copper surface is the transformation of the $CuGa_2$ phase into Cu_9Ga_4 phase. Since there is no $CuGa_2$ phase already at 50°C in this case, this transformation does not occur. The large remaining amount of copper is due to a larger Cu/Ga ratio. It also shows that the composition is stable even with an abundance of copper.

4.4.4.6 Covering with gallium before bonding

The wet chemical treatment to remove the copper oxide just before bonding has the disadvantage that the copper oxide will grow again soon in air soon after the etching. There is literature that claims the effect of copper oxide removal is stable several hours or even days (Rebhan, et al., 2014). During the investigations in this work, such behaviour could not be found; by contrast, it was found that the time between pre-treatment and bonding is critical. After more than 10min in between the two process steps, the bonding yield effectively dropped to zero. To circumvent such time constraint covering copper with an oxidation resistant layer described in the previous part is useful. However, sometimes

in situ sputtering is difficult, depending on the availability of sputter targets and equipment. In such a case, it may be interesting to cover the copper after sputtering with a layer. Before this deposition, the copper oxide obviously needs to be removed. A good possibility for this process is gallium electroplating. The gallium electrolyte has a pH value of >10 and attacks copper oxide and copper. By putting the copper into the electrolyte, the natural copper oxide is automatically removed and it can be covered by a thin gallium layer by electroplating. The gallium is alloying with copper and forming a cover consisting of $CuGa_2$. This cover is protecting the copper from oxidation at air. Simić found that only traces of copper oxide can be found even after one year at air. (Simić, et al., 1998)

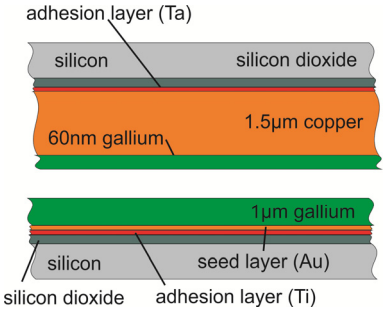


Figure 64. Experimental setup to test the application of a gallium cover layer to prevent the oxidation of copper

The bonding process itself is not different compared to other methods. (25°C, force: 1000N, atmosphere: N_2 1Pa, time 10min). Samples have been prepared according to Figure 64 with 60nm gallium on copper (20s electroplating time).

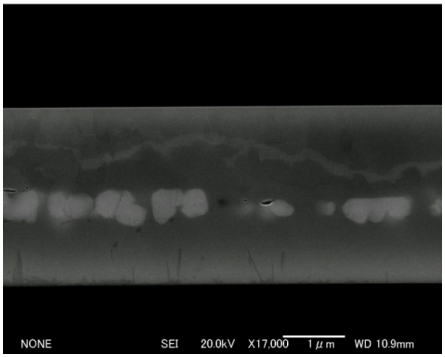


Figure 65. SEM picture of cross section of Cu/Ga bond at 25°C with gallium cover on Cu and annealing at 50°C for 80h

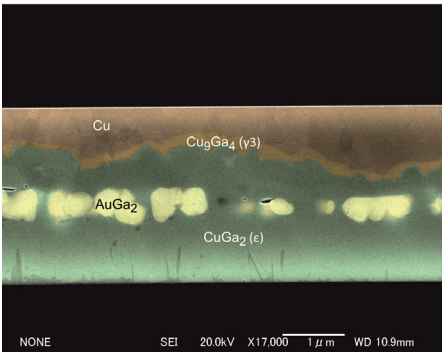


Figure 66. SEM picture of cross section of Cu/Ga bond at 25°C with gallium cover on Cu and annealing at 50°C for 80h, alloy composition highlighted by different colour

The bond result depicted in Figure 65 and Figure 66 shows basically the same composition like a bond interface with wet copper pre-treatment. Inside the $CuGa_2$ phase $AuGa_2$ cluster are visible that are located mainly in the area of the initial interface between copper and gallium. Between $CuGa_2$ and the remaining copper a thin layer of Cu_9Ga_4 exist. Judging from this information the gallium protection layer on top of the copper does not essentially influence the bonding process itself beyond its function to prevent copper oxidation.

4.4.5 Mechanical properties

One of the most important parameters in case of bonding interfaces is the fracture toughness. Typical it is measured by pull test or shear test. In this case, it was decided to use shear test. For all following tests, pairs of oxidised (500nm SiO_2) silicon chips (2cm x 2cm) have been coated with copper respective gallium. The copper was sputtered on top of a tantalum layer using magnetron sputter equipment. Tantalum and copper was sputtered in situ with 300W power and 0.5Pa Ar pressure, sputter time was adjusted to achieve 20nm Ta thickness and 1.2µm copper thickness. 1µm Gallium was deposited by electroplating (see chapter 2.1.3 for parameters and conditions) on a 50nm gold seed layer that was sputtered in situ with 300W, 0.5Pa Ar on a 20nm titanium adhesion layer. Bonding was done for all the sample pairs with the same conditions: 2000N, 25°C, 20min at <1Pa N_2 pressure. The bonding equipment was an EVG 520 commercial wafer bonder. After bonding, the chips have been diced into 5mm x 2.5mm dies. To obtain information on the temperature stability and morphologic changes in the bond interface depended on temperature samples have been annealed at different temperatures (50°C, 90°C, 145° and 200°C) for 80h, after which the shear test took place. For details on the test equipment and test parameters, please refer to chapter 3.1.

4.4.5.1 Cu/Ga bonding without surface pre-treatment

It was decided to include an experiment without copper oxide removal as a reference, although the expected fracture toughness should be very low. Therefore, samples with copper surfaces as sputtered without pre-treatment was used.

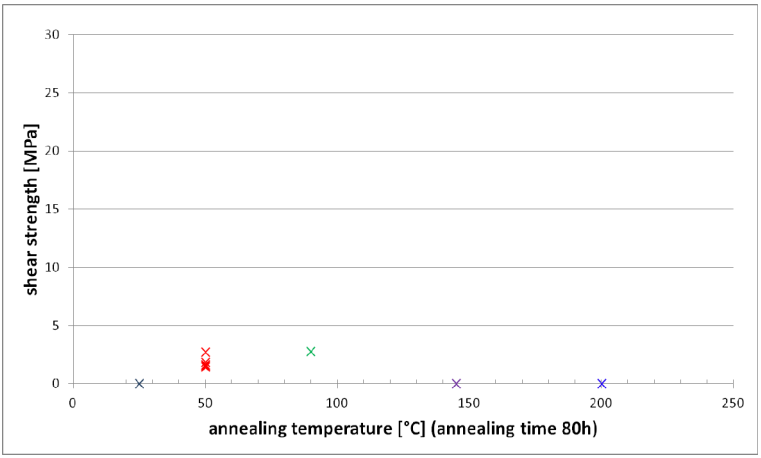


Figure 67. Shear strength of Ga-Cu samples bonded at 25°C without Cu surface treatment and annealed at different temperatures

It already become obvious during dicing that the bonding yield was almost zero. Only a very small number of samples could be obtained for further testing. During the shear test, all remaining samples failed at very low forces, whereby some failed even during handling in preparation of the tests. (Figure 67) An observation of the fracture surface revealed that bonding only happened in very small areas, if at all. The copper surface did not change appearance.

4.4.5.2 Cu/Ga bonding with wet chemical surface pre-treatment

Just before bonding, the copper-coated samples have been dipped into citric acid solution (1wt% concentration) at room temperature for 10s, before rinsing in DI-water (30s) and spin drying happened. The time between this procedure and the bonding was kept within

5min for all samples. The comparatively large yield of more than 80% already became obvious during the dicing. Accordingly, at least ten test samples for all temperature annealing conditions were obtained.

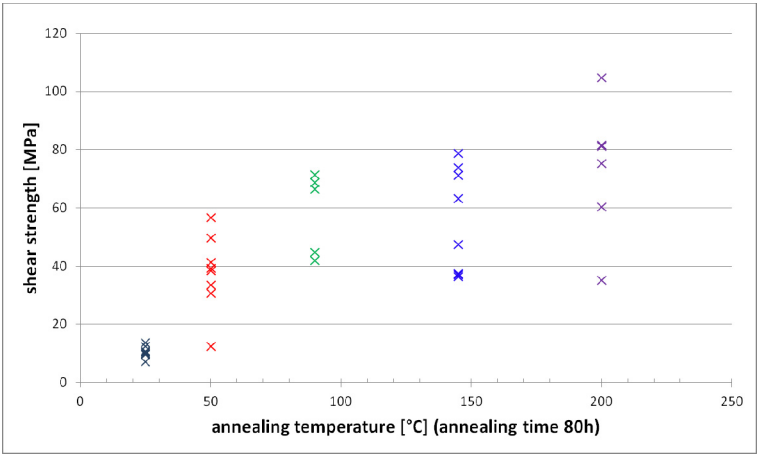


Figure 68. Shear strength of Ga-Cu samples bonded at 25°C with wet Cu surface treatment and annealed at different temperatures

Figure 68 shows the result for every sample. It can be seen that directly after bonding the shear strengths is very small, about 10MPa, but annealing shows an immediate effect. Already at 50°C, the shear strength significantly increases.

Table 16. Average shear strength of samples bonded Cu/Ga at 25°C with citric acid pre-treatment annealed at different temperatures

annealing temperature	average shear strength
-	10.5MPa
50°C	37.8MPa
90°C	58.7MPa
145°	55.7MPa
200°	73.1MPa

As can be seen from Table 16 after annealing at 90°C the average shear strength is higher than 50MPa. Shear strength of higher than 50MPa can be considered as sufficient for even demanding applications, for example glass frit bonds typically have such shear strength (Vogel, et al., 2012).
The dominant failure mode is cohesive failure in the Cu/Ga alloy. The fracture surface shows that the bonding area is not entirely uniform; rather, there are spots that have not

bonded. It may be the case that copper oxide removal and/or oxide regrowth are not uniform and leave areas that already or still have copper oxide.

4.4.5.3 Covering of copper with an gallium layer

After sputtering, the copper has been coated by a 60nm thick layer of gallium. The electrolyte removed the copper oxide by etching during the deposition process. There was no pre-treatment of the samples before bonding. Yield after dicing was higher (>90%) than the samples that have been wet chemical treated. The obtained measurement data shows the same principal behaviour like previous test. (Figure 69)

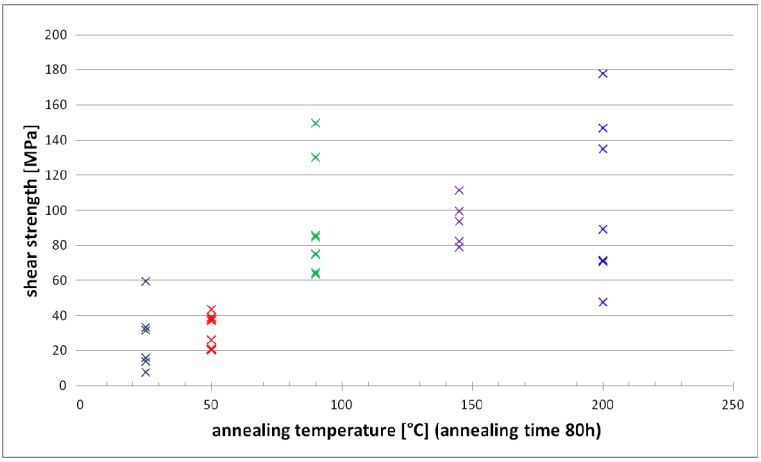


Figure 69. Shear strength of Ga-Cu samples bonded at 25°C with Cu surface protected by electroplated gallium layer and annealed at different temperatures

After annealing at 90°C shear strength becomes high. Actually strength values are much higher. (Table 17) By observing fracture interface and cross sections, the reason for the higher strength is the generally smaller void formation and larger bonded area. Almost no not-bonded area could be observed. The cover with gallium seems an effective counter measure against copper oxide.

Table 17. Average shear strength of samples bonded Cu/Ga at 25°C with gallium cover on copper annealed at different temperatures

annealing temperature	average shear strength
-	27.1MPa
50°C	30.8MPa
90°C	90.2MPa
145°	93.3MPa
200°	105.7MPa

By comparing the different tests also with the results from the Au/Ga bonding, it becomes obvious that Cu/Ga bonding generally has much higher shear strength. (Figure 70) This can be attributed to the extreme formation of voids in case of Au/Ga bonding. The fracture of the bonding area is moving along the voids. Furthermore, it becomes clear that the avoidance of copper oxide also has a considerate impact on the shear strength. This is due to the increase of bonded area with better removal of the oxide. The method to protect the copper surface by a gallium layer shows much better results than the wet chemical treatment.

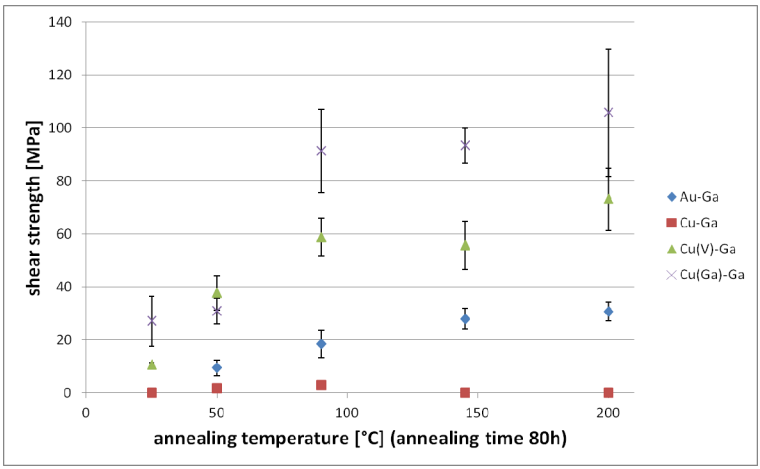


Figure 70. Comparison of shear strength of Ga-Cu samples bonded at 25°C without Cu surface pre-treatment [Cu-Ga], with Cu surface pre-treatment [Cu(V)-Ga] and Cu protected by electroplated gallium layer [Cu(Ga)-Ga], annealed at different temperatures. Furthermore, results from gold-gallium bonding [Au-Ga] are also included for reference.

4.4.6 Electrical properties

Beside the mechanical parameter shear, strength the electric conductivity/resistivity of a bonded contact is of high interest. This is related to the possible application of 3D

integration and stacking of components that require vertical contacts. From the point of understanding the alloying process, observing the change in electrical conductance during the annealing process gives valuable information.
For the measurements sample structures according to chapter 3.2 have been prepared. These samples have been bonded with a commercial wafer bonder EVG 520, all of them with the same parameter, regardless of copper surface treatment: 25°C, 2000N mechanical force, 20min, and <1Pa N_2. After measuring the initial resistance, the samples have been annealed at different temperatures. During the annealing process, electrical resistance of the samples was measured periodically, whereas resistivity was calculated based upon the result.

4.4.6.1 Cu/Ga bonding with wet chemical surface pre-treatment

Just before bonding, the copper-coated samples have been dipped into citric acid solution (1wt% concentration) at room temperature for 10s, before rinsing in DI-water (30s) and spin drying happened. The time between this procedure and the bonding was kept within 5min for all samples.

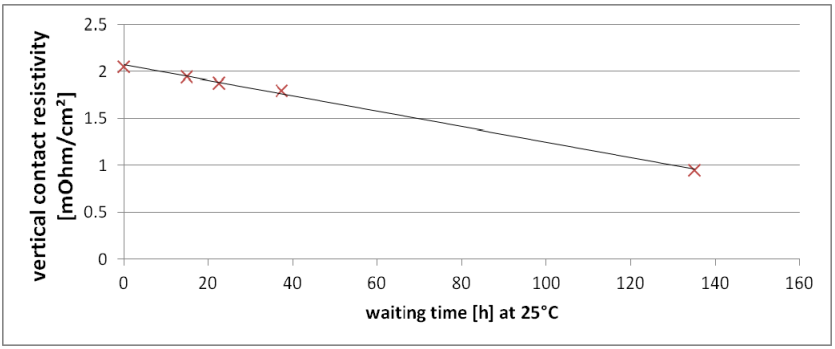


Figure 71. Resistivity of bonded Cu/Ga interface with wet chemical pre-treatment observed over time after bonding at 25°C

The results show that from initial value resistivity dropped to about half its value during observation time. (Figure 71) This is a clear indication that alloying process already starts at room temperature. By annealing at higher temperatures, resistivity further decreases, whereby the minimum value seems to level off at about $3.5x10^{-4}\Omega/cm^2$ after 145°C. (Figure 72)

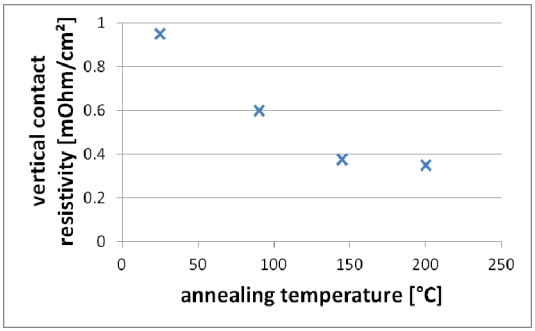


Figure 72. Resistivity of bonded Cu/Ga interface with wet chemical pre-treatment observed over time after bonding at 25°C and annealed at different temperatures

4.4.6.2 Covering of copper with an gallium layer

After sputtering, the copper has been coated by a 60nm thick layer of gallium. The electrolyte removed the copper oxide by etching during the deposition process.
Storage at room temperature reveals a different behaviour compared to the wet chemical treated sample. There is also a decrease in resistivity, but it is much smaller. (Figure 73)

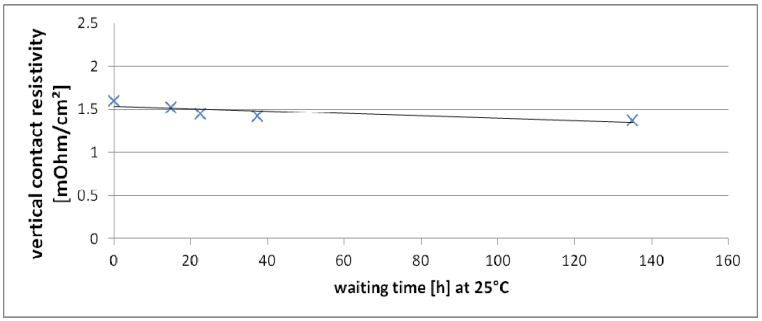


Figure 73. Resistivity of bonded Cu/Ga interface with gallium cover on copper observed over time after bonding at 25°C

When seeing the resistivity change with annealing temperature it becomes obvious that the measurement value levels of at about the same level, $3.5x10^{-4}\Omega/cm2$. (Figure 74) However, the initial value is higher. The gallium that was deposited on top of the copper forms an alloy with the copper. According to the bonding result (yield/shear strength), this alloy is effective in preventing oxidation, although it seems to have the effect of slowing down the diffusion of copper into gallium and vice versa at room temperature. At higher temperatures, the bond interfaces have effectively reached the same morphology and thus reach the same resistivity.

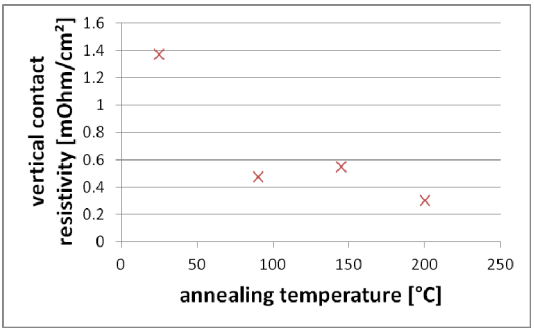


Figure 74. Resistivity of bonded Cu/Ga interface with gallium cover on copper observed over time after bonding at 25°C and annealed at different temperatures.

The minimum achieved resistivity of about $3.5x10^{-4}\Omega/cm^2$ is considerably larger than pure metal contacts. According to existing literature, thermo-compression bonded Cu/Cu can achieve up to about $1x10^{-8}\Omega/cm^2$ resistivity. (Chen, et al., 2004)

4.4.7 Hermeticity

To test the hermetic properties of gallium/copper bonds a test structure with the same design as described in 0 has been used. The process sequence is also similar. The only difference is the use of copper with titanium adhesion layer on the unstructured wafer rather than gold with chromium. The copper and titanium have been sputtered by magnetron sputtering with 300W RF power and 0.5Pa chamber pressure under argon flow. Thickness is 20nm and 1.3µm respectively. Furthermore the gallium thickness has been amended to 1µm. Bonding frame width was 200µm.

A big difference to bonding gallium with gold is the need to apply pre-treatment to copper, as described in 4.4.4. For this experiment, the wafers covered with copper have been dipped in $C_6H_8O_7$ for 1min, rinsed in H_2O and spin dried just before bonding. The time between the copper oxide removal and bonding was kept as short as possible and remained within 5min.

Bonding was done at 7MPa pressure at 50°C for 20min under vacuum condition (0.1Pa N_2), no additional annealing happened. The membrane was visibly detected immediately after bonding. The membrane deflection even remains visible after a long time, namely for more than one year. (Froemel, et al., 2014)

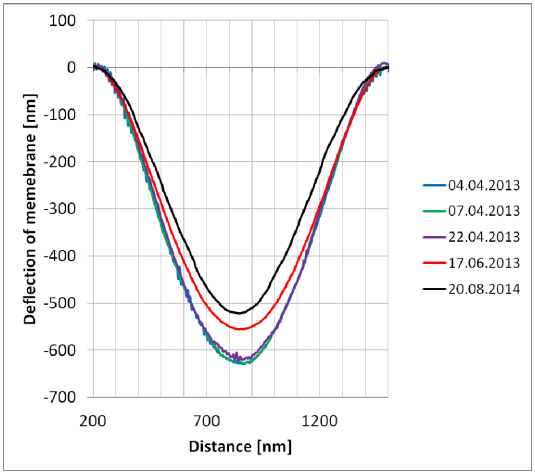


Figure 75. Membrane deflection of hermeticity test structure for gallium/copper bonds measured at different times after bonding. It shows the slow increase of pressure inside of the cavity due to diffusion of air.

As visible in Figure 75 it was clearly measureable that the membrane deflection slowly decreased over time. This makes it possible to calculate the leak rate as described in chapter 3.3.1 and formula 10. Parameters used for the calculation are shown in Table 18.

Table 18: Parameters used for calculation of leak rate using membrane deflection of bonded gallium/copper samples

parameter	value	explanation
Δh	0.11x10-6m	difference in centre membrane deflection
tm	0.65x10-6m	membrane thickness
a	2.57x10-3m	half width of membrane side length
V	11.5x10-8m³	volume of cavity

The calculation of the leak rate results in $1.5x10^{-13}$Pa m³/s. According to MIL-STD 833J, a package with internal volume smaller than $5x10^{-6}$m³ is considered hermetic tight in case the leak rate is smaller than $5.07x10^{-7}$Pa m³/s. The measurement results for gallium/copper bonds with the given parameters show that this condition is fulfilled and it can be considered hermetic.

4.4.8 Summary and discussion Cu/Ga bonding

To form a comprehensive theory, all temperature dependant test results need to be compared, checked for validity and interpreted. This is done with the example of samples with copper covered with gallium. (Figure 76)

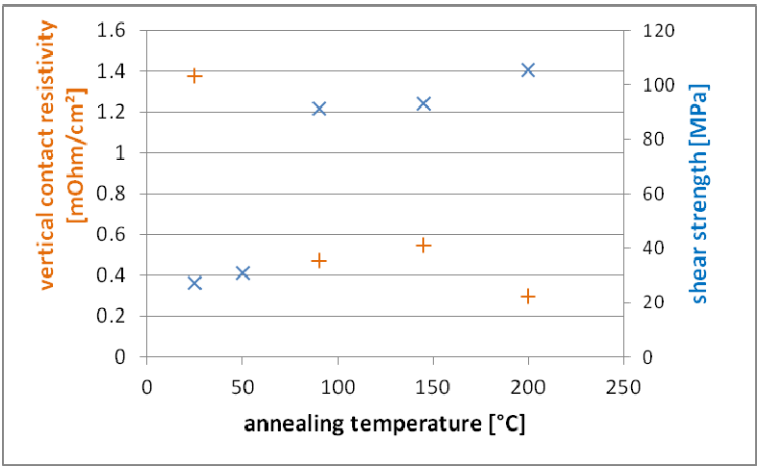


Figure 76. Overview of mechanical and electrical parameters of Cu/Ga bonded interface depending on annealing temperature.

It is obvious upon first glance that the mechanical and electrical measurement data fits very well together. Two trends can be observed. At 90°C shear strength increases threefold and vertical contact resistance becomes about 2.5 times smaller. By annealing at 200°C, another improvement is visible, albeit significantly smaller. From the investigation of interface composition in dependence of annealing temperature (chapter 4.3.3), an explanation for both phenomenons can be found. The most obvious structural difference between the interfaces annealed at 50°C and 90°C is the existence of an uninterrupted layer of Cu_9Ga_4 phase in between Cu intermetallic phase and $CuGa_2$ phase after annealing at 90°C. Obviously, the Cu_9Ga_4 interlayer is very important to achieve good bonding parameters. The second trend, the improvement at 200°C, can be attributed to the elimination of the $CuGa_2$ phase and its replacement by the γ1-phase that forms a uniform interface with included $AuGa_2$ clusters.
The volume change during alloying process has been investigated by calculation of molar volumes of reaction products and educts.

Table 19: molar volume of selected phases Au/Ga binary system

material	molar volume
Cu	7.12cm³/mol
Cu_9Ga_4	99.74cm³/mol
$CuGa_2$	28.15cm³/mol
Ga	10.58cm³/mol

By comparing the molar volume of $CuGa_2$ with the molar volume (Table 19) of gallium and copper (2 mol gallium and 1 mol Cu), it can be seen that 0.2% of the volume shrinks. 1 mol of Cu_9Ga_4 comprises 9 mol Cu and 4 mol Ga. Together, the gallium and copper required for 1 mol of Cu_9Ga_4 have a volume of 106.4cm³, equalling a shrinkage of 6.26%, which is very similar to Cu/Sn (Cu_6Sn_5) bonding with 6.83% shrinkage.

In chapter 4.4, investigations about alloying between copper and gallium for semiconductor wafer bonding have been described. Wafer bonds have been successfully achieved at room temperature, although shear strength was relatively low without additional annealing. Observation of interfaces after bonding revealed that first $CuGa_2$ is formed and gallium is entirely used up during the alloying process. With annealing, it gradually changes to Cu_9Ga_4 by consuming copper. This behaviour matches very well with experimental observations of other researchers that investigated copper/gallium alloying (Lin, et al., 2013). High shear strength was obtained by annealing at 90°C after bonding. Annealing at 200°C achieved a stable interface composition of Cu_9Ga_4 with embedded $AuGa_2$ clusters that have formed from the seed layer of gallium electroplating. It was shown that copper pre-treatment is essential for successful bonding and several successful methods (wet chemical etching, gold cover on copper, and gallium cover on copper) for this pre-treatment were demonstrated. Furthermore, hermeticity of copper-gallium bonds, bonded at 50°C, could be proven. (Froemel, et al., 2013)

4.5 Discussion of void formation

One of the most important phenomenon observed in these investigations is the void formation. In both material systems Au/Ga and Cu/Ga the formation of voids has been observed. Voids have a very large influence on the properties of the bonded interface. They reduce strength, because cracks can propagate easily along them; they reduce the electric conductance, because the effective conductive area is reduced; and hermetic properties are worsened, because the voids open paths for gas transport in the interface. That large importance justifies detailed discussion.
One possible reason for void formation is volume shrinkage during the process. This effect has been calculated in the previous respective chapters and found to be existent, although it the quantity found it does not explain the extensive formation of voids by itself alone, especially in the case of Au/Ga. The main responsible effect has to be found in the

diffusion process itself. As has been explained in 4.1, interdiffusion is described by the interdiffusion coefficient, $\widetilde{D}$, which is a common property of both diffusion partners and does not yield information about the individual behaviour of each alloying partner. More than 60 years ago, Kirkendall made experiments to understand the contribution of the individual elements to the overall diffusion. (Smigelskas, et al., 1947) Up to that point, the common knowledge was that diffusion is happening by exchange of atoms with the respective other element. However, he found that diffusion in solid state is mainly mandated by vacancy movement and subsequently is characterised by real material transport. What does this mean for practical purpose? At an interface between two elements, there will be diffusion by element A into element B (D_A) and element B into element A (D_B). (Figure 77)

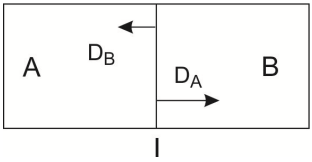


Figure 77. Diffusion streams D_A and D_B at the interface between elements A and B

In almost all cases is $D_B \neq D_A$. If one of the interdiffusion coefficients is much larger than the other voids remain in the volume of the element with higher mobility. It is accepted nowadays that this Kirkendall Effect is responsible for void formation in soldering, e.g. Cu/Sn. The voids that are created by this effect are consequently called Kirkendall Voids.
In systems with many different phases, the effect can happen at each interface.
Figure 78 shows the situation during Au/Ga alloying. Unfortunately, to the author's best knowledge the individual diffusion coefficients at each interface for the gold-gallium as well as copper-gallium combination have not yet been investigated. The diffusion coefficients can be experimentally investigated by adding radioactive markers into the interface, for example. With the knowledge of the individual diffusion coefficients, it would have been possible to show the Kirkendall Effect quantitative, although the experimental determination of them was beyond the scope of this work.

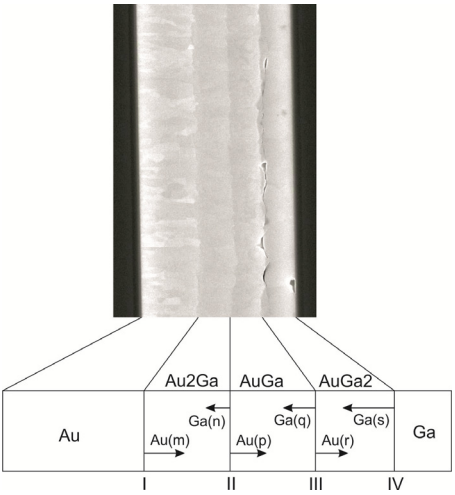


Figure 78. Interfaces and diffusion on the example of Au/Ga

In case of copper/gallium, it was possible to show the effect qualitative. For a sample pair, copper-gallium the copper surface area was treated partially with citric acid directly before bonding, by applying the citric acid with a brush. The result of this is that the direct vertical diffusion was inhibited in defined areas. Therefore, in the vertical diffusion inhibited area, further alloying can only occur by horizontal diffusion. This allows sufficient time to prepare cross section and observe it before all gallium is used up to form $CuGa_2$, thus giving the opportunity to investigate movement of the $CuGa_2$/Cu interface. In Figure 79 and Figure 80 the effect can be seen optically. The cross section originally has been made by ion cutting. The picture in Figure 80 has been taken 88h hours after the picture Figure 79 without any treatment and shows the diffusion effect at room temperature.

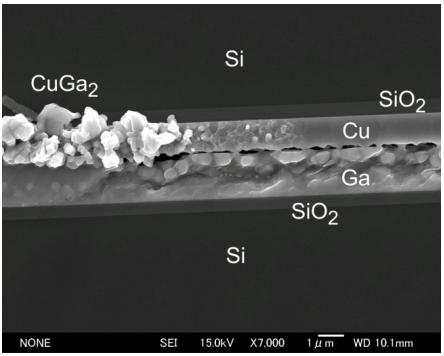


Figure 79. SEM cross section of bonded copper-gallium pair; dashed line shows interface with inhibited diffusion

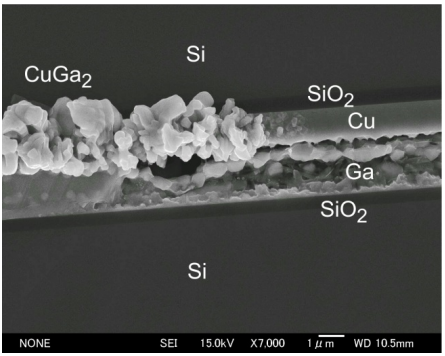


Figure 80. SEM cross section of same sample and position like Figure 79, taken 88h later (no annealing, room temperature!);visible increase of $CuGa_2$ phase and void formation in the gallium layer

The interface $CuGa_2$/Cu (Cu_9Ga_4) is moving to Cu, and consequently voids are formed in the gallium layer. This is a clear sign that gallium has a higher mobility in copper and in the intermetallic phases than copper has. Similar results can be observed in other systems like gold/indium where indium has higher mobility than gold (Welch III, et al., 2005).

5. Summary

In this chapter, important points themed in this work shall be discussed and summarised. The motivation for this work was the need to increase the portfolio of available semiconductor bonding technologies with methods that allow bonding at or near room temperature with metallic interfaces. These technologies are needed to fabricate and package micro devices with heterogeneous, temperature sensible materials. Whereas such methods essentially already exist, every technology has constraints that limits its applicability. This background has been described in chapter 1. Bonding by SLID is now an accepted technology (Cu/Sn) in the semiconductor industry. There are established methods, standards and equipment in industrial applications available. By changing only the material while using the same basic principle, at least some of the methods, standards and equipment can be adopted. To have a very low bonding temperature, it was decided to use gallium as bonding partner. One of the key points for application is a suitable deposition method for it, given that there is not yet an established technology to deposit gallium on semiconductor substrates. It was possible to show in this work that electroplating based upon gallium chloride can be used for deposition. The electroplating was characterised and successfully applied to bonding samples. The developed technique allows repeatable electroplating of thin films with defined thickness on a variety of seed layers. Beside the deposition also the structuring of the gallium and the seed layer could be successfully tested. This is an essential prerequisite for the bonding itself. In chapter 2 this information can be found. Regarding the bonding, two material combinations have been investigated, namely Au/Ga and Cu/Ga. The result of the investigations showed both combinations to be applicable, albeit with different set of advantages and disadvantages. Au/Ga does not require any surface pre-treatment prior to bonding in contrast to Cu/Ga. Cu/Ga on the other hand side yields higher bonding strength, lower electric resistance and possibility for hermetic bonding. For both methods, the interface characteristic in dependence of temperature has been investigated and the temperature dependence of bonding strength as well as resistance could be traced back to the interface composition. In both material combinations, bonding at room temperature was possible, although annealing least 90°C was necessary to achieve stable conditions. Chapter 4 holds the extensive information about the bonding experiments and their results. The characterization techniques used are described in chapter 3.

Due to the extensive void formation problem, bonding of gold and gallium has only limited applicability. On the other hand, copper/gallium bonding is highly interesting. High shear strength, acceptable conductivity and very good hermeticity could be achieved. All needed process steps: gallium deposition, gallium structuring and bonding have been developed, successfully demonstrated and characterised. Accordingly, with the results obtained, the ground has been paved to apply this bonding technology for real devices and applications. That should be the next step in the way of using the developed knowledge.

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